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# **CMOS linear image sensor**

S13488-01

## High sensitivity (with a gain switch function)

The S13488-01 is a high sensitivity CMOS linear image sensor employing a photosensitive area of  $14 \times 42 \mu m$  pixel size. It features lower noise and higher sensitivity (with a gain switch function) than the previous product (S11638).

#### Features

- Pixel size: 14 × 42 µm
- 2048 pixels
- Effective photosensitive area length: 28.672 mm
- High sensitivity: with a gain switch function [1100 V/(lx·s)]
- Spectral response range: 400 to 1000 nm
- Simultaneous charge integration for all pixels
- **Variable integration time function (electronic shutter function)**
- **5** V single power supply operation
- Built-in timing generator allows operation with only start and clock pulse inputs
- Video data rate: 10 MHz max.

#### Applications

- Spectrometers
- Position detection
- Image reading
- **Encoders**

#### Structure

Parameter	Specification	Unit
Number of pixels	2048	-
Pixel size	14 × 42	μm
Photosensitive area length	28.672	mm
Package	LCP (liquid crystal polymer)	-
Window material	Borosilicate glass	-

#### Absolute maximum ratings

Parameter	Symbol	Condition	Value	Unit
Supply voltage	Vdd	Ta=25 °C	-0.3 to +6	V
Clock pulse voltage	V(CLK)	Ta=25 °C	-0.3 to +6	V
Start pulse voltage	V(ST)	Ta=25 °C	-0.3 to +6	V
Gain selection terminal voltage	Vg	Ta=25 °C	-0.3 to +6	V
Operating temperature	Topr	No dew condensation*1	-40 to +85	°C
Storage temperature	Tstg	No dew condensation*1	-40 to +85	°C

\*1: When there is a temperature difference between a product and the surrounding area in high humidity environment, dew condensation may occur on the product surface. Dew condensation on the product may cause deterioration in characteristics and reliability.

Note: Exceeding the absolute maximum ratings even momentarily may cause a drop in product quality. Always be sure to use the product within the absolute maximum ratings.

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### Recommended terminal voltage (Ta=25 °C)

Parameter		Symbol	Min.	Тур.	Max.	Unit
Supply voltage		Vdd	4.75	5	5.25	V
	High level		3	Vdd	Vdd + 0.25	V
Clock pulse voltage	Low level	V(CLK)	0	-	0.3	V
Start pulso voltago	High level	V(ST)	3	Vdd	Vdd + 0.25	V
Start pulse voltage	Low level	V(ST)	0	-	0.3	V
Gain selection	High gain	Va	0	-	0.3	V
terminal voltage	Low gain	Vg	3	Vdd	Vdd + 0.25	V

## Input terminal capacitance (Ta=25 °C, Vdd=5 V)

Parameter	Symbol	Min.	Тур.	Max.	Unit
Clock pulse input terminal capacitance	C(CLK)	-	5	-	pF
Start pulse input terminal capacitance	C(ST)	-	5	-	pF
Gain selection terminal capacitance	C(Vg)	-	5	-	pF

#### Electrical characteristics [Ta=25 °C, Vdd=5 V, V(CLK)=V(ST)=5 V]

Parameter	Symbol	Min.	Тур.	Max.	Unit
Clock pulse frequency	f(CLK)	200 k	-	10 M	Hz
Video data rate	VR	-	f(CLK)	-	Hz
Output impedance	Zo	70	-	260	Ω
Current consumption*2 *3 High gain	Ic	60	75	100	m۸
Low gain	IC	20	35	60	mA

\*2: f(CLK)=10 MHz

\*3: Current consumption increases as the clock pulse frequency increases. The current consumption is 55 mA (high gain), 15 mA (Low gain) at f(CLK)=200 kHz.



## Electrical and optical characteristics [Ta=25 °C, Vdd=5 V, V(CLK)=V(ST)=5 V, f(CLK)=10 MHz]

Parameter		Symbol	Min.	Тур.	Max.	Unit
Spectral response range		λ	400 to 1000			nm
Peak sensitivity waveleng	gth	λp	-	700	-	nm
Dhataaanaitii iitii i*4	High gain		-	1350	-	
Photosensitivity*4	Low gain	Sw	-	270	-	$V/(lx \cdot s)$
Conversion officiency*5	High gain	CF	-	125	-	
Conversion efficiency*5	Low gain	CE	-	25	-	µV/e⁻
Dark output voltage*6	High gain	1/0	0	1.5	15	m\/
Dark output voltage*6	Low gain	VD	0	0.1	2	mV
Saturation output	High gain	Vsat	3.5	4	4.5	V
voltage*7	Low gain		1.5	2	2.5	V
Readout noise*8	High gain	Nurad	0.1	0.9	2	m)/ mm c
Reduout noise"	Low gain	Nread	0.1	0.4	1.2	mV rms
· ····································	High gain	DR1	-	4444	-	times
Dynamic range 1*9	Low gain	DKI	-	5000	-	umes
Dunamia rango 2×10	High gain	500	-	2600	-	timos
Dynamic range 2 <sup>*10</sup>	Low gain	DR2	-	20000	-	times
Output offset voltage		Voffset	0.4	0.6	1	V
Photoresponse nonunifor	Photoresponse nonuniformity*4 *11		-	±2	±10	%
Image lag*12		Lag	-	-	0.1	%

\*4: Measured with a tungsten lamp of 2856 K

\*5: Output voltage generated per one electron

\*6: Integration time=10 ms

\*7: Difference from Voffset

\*8: When a capacitor of about 1  $\mu\text{F}$  is inserted between IBIAS1 and GND and between IBIAS2 and GND.

\*9: DR1= Vsat/Nread

\*10: DR2= Vsat/VD

Integration time=10 ms

Dark output voltage is proportional to the integration time and so the shorter the integration time, the wider the dynamic range.

\*11: Photoresponse nonuniformity (PRNU) is the output nonuniformity that occurs when the entire photosensitive area is uniformly illuminated by light which is 50% of the saturation exposure level. PRNU is measured using 2042 pixels excluding 3 pixels each at both ends, and is defined as follows:

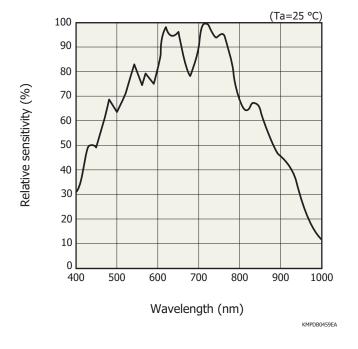
 $\mathsf{PRNU} = \Delta X / X \times 100 \ (\%)$ 

X: average output of all pixels,  $\Delta X$ : difference between X and maximum output or minimum output

\*12: Signal components of the preceding line data that still remain even after the data is read out in a saturation output state.

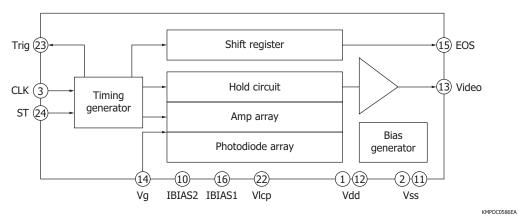
Image lag increases when the output exceeds the saturation output voltage.





## Spectral response (typical example)

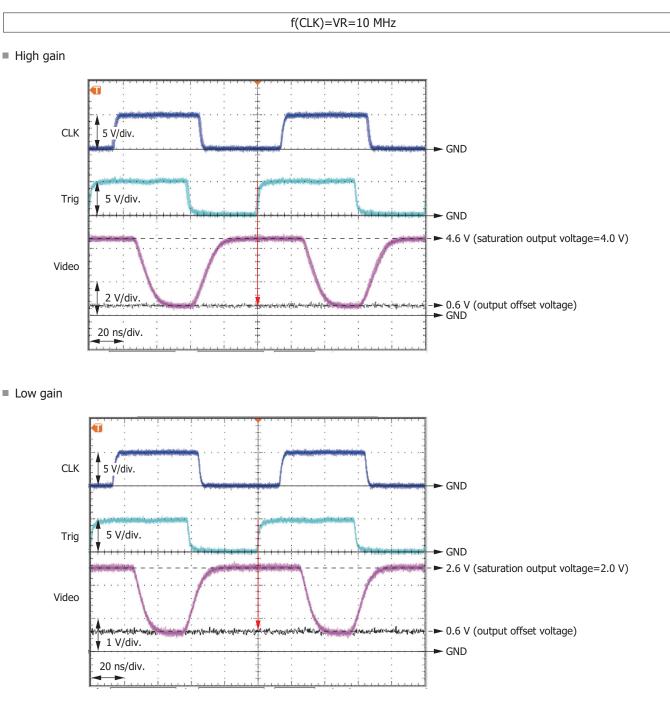
## Block diagram



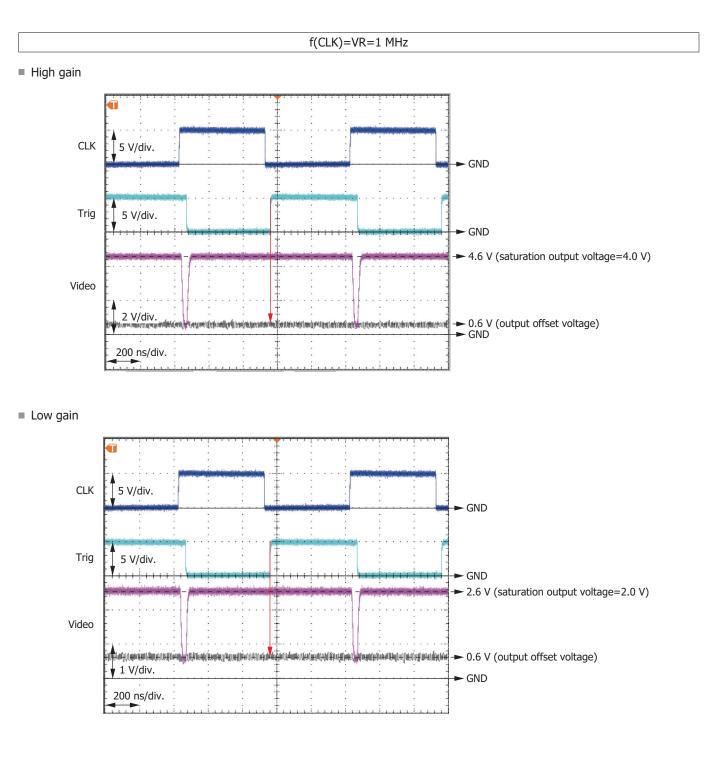


## Output waveform of one pixel

The timing for acquiring the Video signal is synchronized with the rising edge of a trigger pulse.

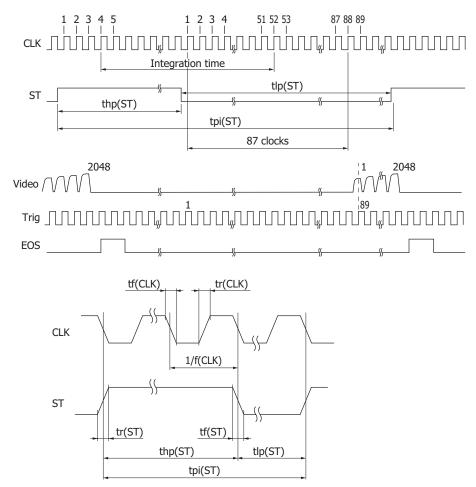








## Timing chart



KMPDC0399EB

Parameter	Symbol	Min.	Тур.	Max.	Unit
Start pulse width interval*13	tpi(ST)	106/f(CLK)	-	-	S
Start pulse high period*13 *14	thp(ST)	6/f(CLK)	-	-	S
Start pulse low period	tlp(ST)	100/f(CLK)	-	-	S
Start pulse rise and fall times	tr(ST), tf(ST)	0	10	30	ns
Clock pulse duty	-	45	50	55	%
Clock pulse rise and fall times	tr(CLK), tf(CLK)	0	10	30	ns

\*13: Dark output increases if the start pulse period or the start pulse high period is lengthened.

\*14: The integration time equals the high period of ST plus 48 CLK cycles.

The shift register starts operation at the rising edge of CLK immediately after ST goes low.

The integration time can be changed by changing the ratio of the high and low periods of ST.

If the first Trig pulse after ST goes low is counted as the first pulse, the Video signal is acquired at the rising edge of the 89th Trig pulse.



## Operation example

When the clock pulse frequency is maximized (video data rate is also maximized), the time of one scan is minimized, and the integration time is maximized (for outputting signals from all 2048 channels)

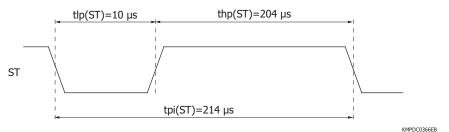
Clock pulse frequency = Video data rate = 10 MHz

Start pulse cycle = 2140/f(CLK) = 2140/10 MHz = 214  $\mu s$ 

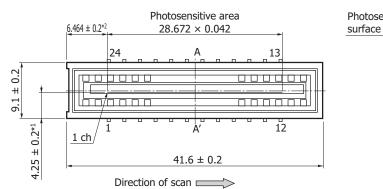
High period of start pulse = Start pulse cycle - Start pulse's low period min.

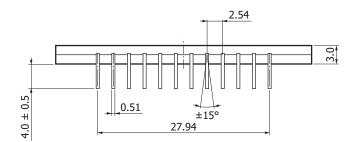
= 2140/f(CLK) - 100/f(CLK) = 2140/10 MHz - 100/10 MHz = 204 μs

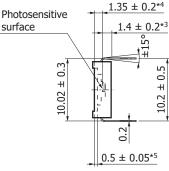
Integration time is equal to the high period of start pulse + 48 cycles of clock pulses, so it will be  $204 + 4.8 = 208.8 \ \mu s$ .



#### Dimensional outline (unit: mm)







A-A' cross section

Tolerance unless otherwise noted: ±0.1 \*1: Distance from package edge

- to photosensitive area center \*2: Distance from package edge
- to photosensitive area edge

\*3: Distance from package bottom to photosensitive surface

- \*4: Distance from window upper surface to photosensitive surface
- \*5: Glass thickness

KMPDA0327EB



#### Pin connections

Pin no.	Symbol	I/O	Description	Pin no.	Symbol	I/O	Description
1	Vdd	I	Supply voltage	13	Video	0	Video signal* <sup>15</sup>
2	Vss		GND	14	Vg	I	Gain selection terminal* <sup>16</sup>
3	CLK	I	Clock pulse	15	EOS	0	End of scan
4	NC		No connection	16	IBIAS1	0	No connection <sup>*17</sup>
5	NC		No connection	17	NC		No connection
6	NC		No connection	18	NC		No connection
7	NC		No connection	19	NC		No connection
8	NC		No connection	20	NC		No connection
9	NC		No connection	21	NC		No connection
10	IBIAS2	0	No connection*17	22	Vlcp	0	Bias voltage for negative voltage circuit <sup>*18</sup>
11	Vss		GND	23	Trig	0	Trigger pulse for video signal acquisition
12	Vdd	I	Supply voltage	24	ST	I	Start pulse

\*15: Connect a buffer amplifier for impedance conversion to the video output terminal so as to minimize the current flow. As the buffer amplifier, use a high input impedance operational amplifier with JFET or CMOS input.

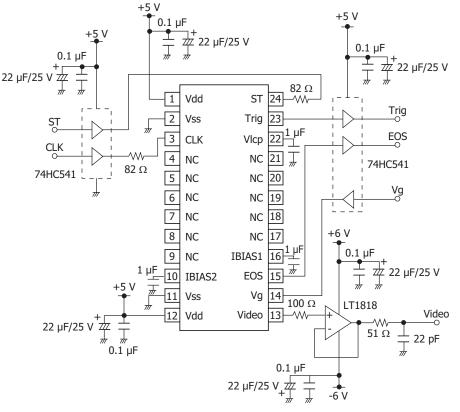
\*16: Select NC or Vdd for low gain and GND for high gain.

\*17: Approximately 1.1 V generated by the voltage circuit inside the chip is output to these terminals. In addition, insert a capacitor of about 1 μF between IBIAS1 and GND and between IBIAS2 and GND. If you are not going to insert these capacitors, be sure to leave these terminals open. In this case, the readout noise is increased to 1.5 mV rms (high gain).

\*18: Approximately -1.5 V generated by the negative voltage circuit inside the chip is output to the terminal. To maintain the voltage, insert a capacitor around 1 µF between Vlcp and GND.

Note: Leave the "NC" terminals open and do not connect them to GND.

#### Application circuit example



KMPDC0587EA



#### Precautions

#### (1) Electrostatic countermeasures

This device has a built-in protection circuit against static electrical charges. However, to prevent destroying the device with electrostatic charges, take countermeasures such as grounding yourself, the workbench and tools to prevent static discharges. Also protect this device from surge voltages which might be caused by peripheral equipment.

#### (2) Light input window

If dust or dirt gets on the light input window, it will show up as black blemishes on the image. When cleaning, avoid rubbing the window surface with dry cloth or dry cotton swab, since doing so may generate static electricity. Use soft cloth, paper or a cotton swab moistened with alcohol to wipe dust and dirt off the window surface. Then blow compressed air onto the window surface so that no spot or stain remains.

#### (3) Soldering

To prevent damaging the device during soldering, take precautions to prevent excessive soldering temperatures and times. Soldering should be performed within 5 seconds at a soldering temperature below 260 °C.

#### (4) Operating and storage environments

Always observe the rated temperature range when handling the device. Operating or storing the device at an excessively high temperature and humidity may cause variations in performance characteristics and must be avoided.

(5) UV exposure

This product is not designed to prevent deterioration of characteristics caused by UV exposure, so do not expose it to UV light.

## Related information

www.hamamatsu.com/sp/ssd/doc en.html

- Precautions
- · Disclaimer
- · Image sensors

Information described in this material is current as of May 2019.

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