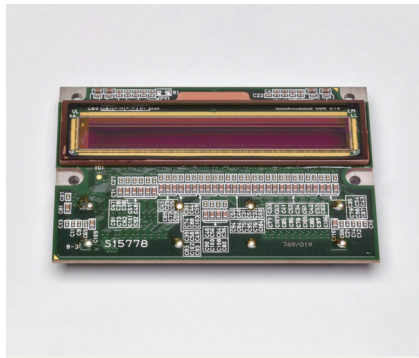# CMOS linear image sensor

S15778

High-speed readout (100 klines/s)

The S15778 is a CMOS linear image sensor developed for industrial cameras that require high-speed scanning. The column-parallel readout system, which has a readout amplifier and an A/D converter for each pixel, allows high-speed readout. For the A/D converter resolution, either 10-bit (high-speed mode: 100 klines/s max.) or 11-bit (low-speed mode: 50 klines/s max.) can be selected. Video signal is output serially in 360 MHz LVDS format.

⊡ Features

- ➔ **Pixel size: 7 × 7 µm**
- ➔ **Number of pixels: 8192**
- ➔ **High-speed readout: 100 klines/s**
- ➔ **Simultaneous integration of all pixels**
- ➔ **3.3/1.8 V power supply operation**
- ➔ **SPI communication function**
- ➔ **Built-in 10-bit/11-bit A/D converters**

⊡ Applications

- ➔ **Machine vision**
- ➔ **Film inspection**
- ➔ **Printed circuit board appearance inspection**
- ➔ **Print inspection**

⊡ Structure

Parameter	Specification	Unit
Number of pixels	8192	-
Pixel pitch	7	µm
Pixel height	7	µm
Effective photosensitive area length	57.344	mm
Package	Glass epoxy and FeNiCo alloy	-
Window material*1	Borosilicate glass	-

*1: AR coated (1% or less reflectance at 400 to 800 nm)

⊡ Absolute maximum ratings (Ta=25 °C)

Parameter		Symbol	Condition	Value	Unit
Supply voltage	Analog terminal	Vdd(A)		-0.3 to +3.9	V
	Digital terminal	Vdd(D)		-0.3 to +3.9	V
	Counter terminal	Vdd(C)		-0.3 to +3.9	V
Digital input signal terminal voltage*2		Vi		-0.3 to +3.9	V
Operating temperature		Topr	No dew condensation*3	-5 to +70	°C
Storage temperature		Tstg	No dew condensation*3	-10 to +70	°C

*2: CS, SCLK, MOSI, RSTB, MCLK, MST, All-reset, PLL-reset

*3: When there is a temperature difference between a product and the surrounding area in high humidity environments, dew condensation may occur on the product surface. Dew condensation on the product may cause deterioration in characteristics and reliability.

Note: Exceeding the absolute maximum ratings even momentarily may cause a drop in product quality. Always be sure to use the product within the absolute maximum ratings.

Recommended operating conditions (Ta=25 °C)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Analog terminal	Vdd(A)	3.15	3.3	3.45	V
	Digital terminal	Vdd(D)	3.15	3.3	3.45	
	Counter terminal	Vdd(C)	1.7	1.8	1.9	
Digital input voltage	High level	Vi(H)	3	Vdd(D)	Vdd(D) + 0.25	V
	Low level	Vi(L)	0	-	0.3	

Electrical characteristics

Digital input signals

[Ta=25 °C, Vdd(A)=Vdd(D)=3.3 V, Vdd(C)=1.8 V]

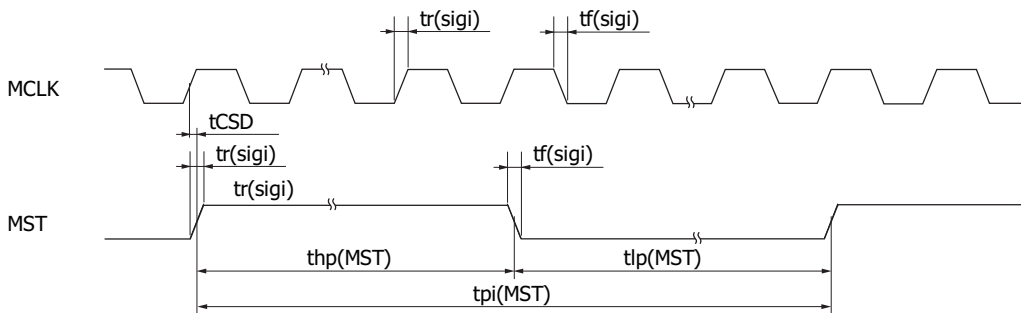| Parameter		Symbol	Min.	Typ.	Max.	Unit
Master clock pulse frequency		f(MCLK)	29	30	31	MHz
Master clock pulse duty cycle		D(MCLK)	45	50	55	%
Master start pulse cycle*4	High-speed mode	tpi(MST)	300/f(MCLK)	-	-	s
	Low-speed mode		600/f(MCLK)	-	-	
Master start pulse high period*4	High-speed mode	thp(MST)	166/f(MCLK)	-	-	s
	Low-speed mode		332/f(MCLK)	-	-	
Master start pulse low period*4	High-speed mode	tlp(MST)	2/f(MCLK)	-	-	s
	Low-speed mode		4/f(MCLK)	-	-	
Delay between master clock and master start		tCSD	-	-	5	ns
Delay between master clock and reset*5		tCRD	-	-	5	ns
Rise time*6		tr(sigi)	-	5	7	ns
Fall time*6		tf(sigi)	-	5	7	ns

*4: The maximum line rate is 100 klines/s in high-speed mode. Line rate is 100 klines/s when tpi(MST) = 300/f(MCLK).
   The maximum line rate is 50 klines/s in low-speed mode. Line rate is 50 klines/s when tpi(MST) = 600/f(MCLK).
*5: Delay time for the rising edge of MCLK and those of PLL_Reset and All_Reset
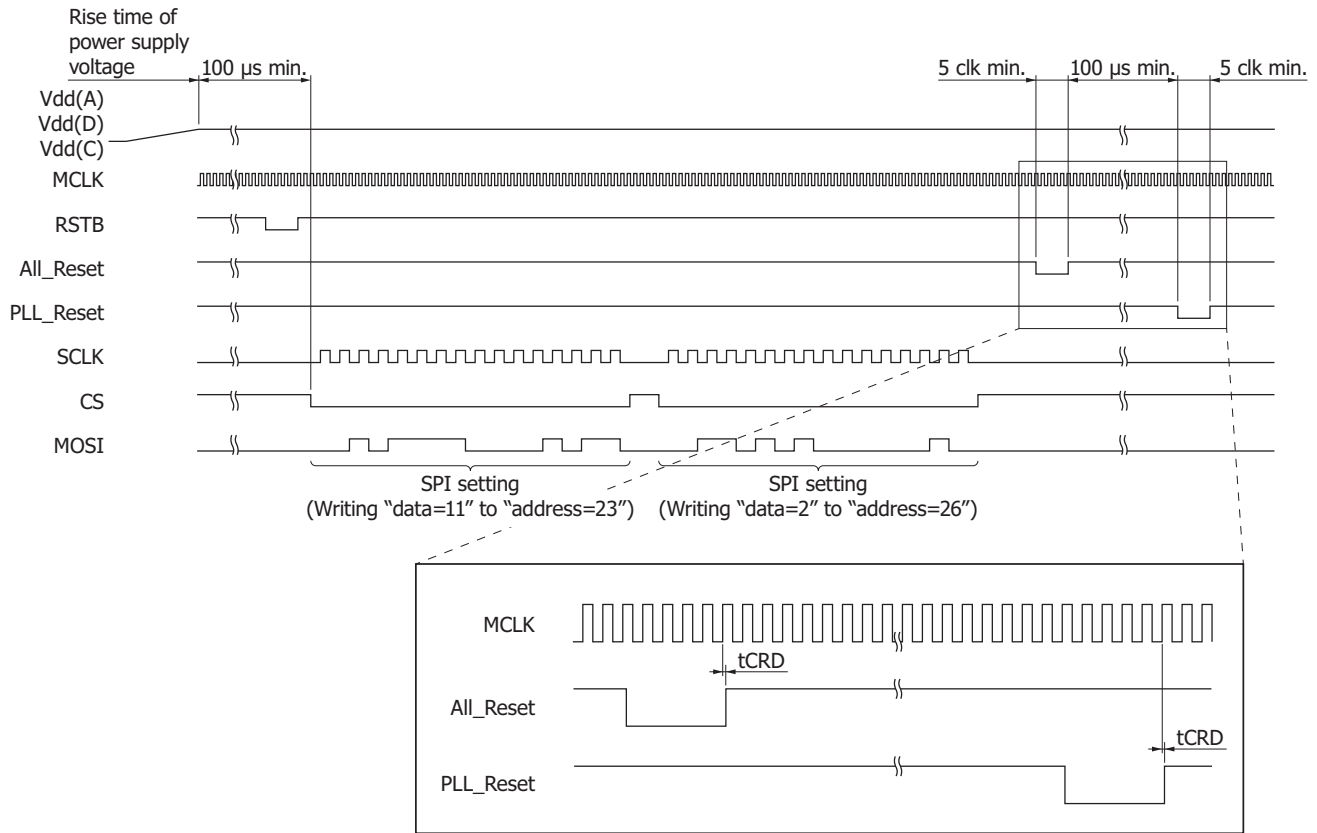*6: Time for the input voltage to rise or fall between 10% and 90%

■ MCLK and MST input timings

KMPDC0677EA

■ SPI setting (address=23, 26), RSTB, PLL_Reset, All_Reset input timings

After turning on the power (100 μs or later), set the SPI. Start inputting MCLK before setting SPI (100 μs or earlier). Set RSTB once to low from starting MCLK until setting SPI. After that, set All_Reset to low level for at least 5 master clock cycles and then do the same for PLL_Reset. Set at least 100 μs between All_Reset and PLL_Reset.

KMPDC0888EB

Digital output signals

[Ta=25 °C, Vdd(A)=Vdd(D)=3.3 V, Vdd(C)=1.8 V, f(MCLK)=30 MHz]

Parameter		Symbol	Min.	Typ.	Max.	Unit
Video data rate (LVDS)		DR	f(MCLK) × 12			MHz
Line rate	High-speed mode	LR	-	-	100	klines/s
	Low-speed mode		-	-	50	
LVDS output voltage[*7]	Offset	Vcom	1.13	1.25	1.38	V
	Differential	Vdiff	0.25	0.35	0.45	
LVDS rise time[*8]		tr(LVDS)	-	0.9	1.3	ns
LVDS fall time[*8]		tf(LVDS)	-	0.9	1.3	ns
Delay between Pclk1 and OutA[m][*9]		tPDD	-0.8	0.1	1	ns
Delay between Pclk1 and CTR1[*9]		tPDC	-0.75	0.15	1.05	ns
Delay between Pclk1 and frame sync signal[*9]	Rise time	tPDSR	-1.35	-0.45	0.55	ns
	Fall time	tPDSF	-1.35	-0.45	0.55	
CMOS output voltage	High	Vsigo(H)	Vdd(D) - 0.25	Vdd(D)	-	V
	Low	Vsigo(L)	-	0	0.25	
Clock pulse frequency of timing generator	High-speed mode	f(TGCLK)	-	f(MCLK)	-	MHz
	Low-speed mode		-	f(MCLK)/2	-	
CMOS output rise time[*10]		tr(sigo)	-	10	12	ns
CMOS output fall time[*10]		tf(sigo)	-	10	12	ns
Delay between bit output sync signal 1 and bit output sync signal 3[*11]		tPDP	5.0	5.8	6.6	ns
Delay between pixel output sync signal 1 and pixel output sync signal 3[*12]		tCDC	5.0	5.8	6.6	ns
Output delay between ports		tDDD	0.65	0.75	0.85	ns

*7: Attach a 100 Ω terminator to the LVDS output terminal.
*8: Time for the output voltage to rise or fall between 10% and 90% when there is a 2 pF load capacitor attached to the output terminal
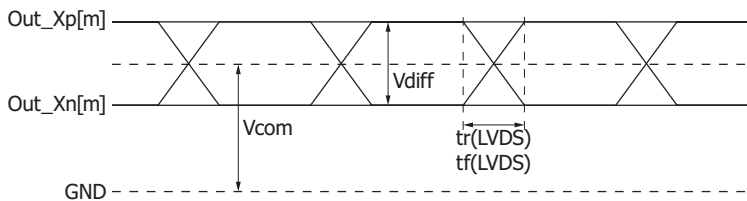*9: Pclk1_delay=0, CTR1_delay=0 [For Pclk and CTR, length of delay can be adjusted by setting SPI.: see SPI address setting (P.14)]
*10: Time for the output voltage to rise or fall between 10% and 90% when there is a 10 pF load capacitor attached to the output terminal
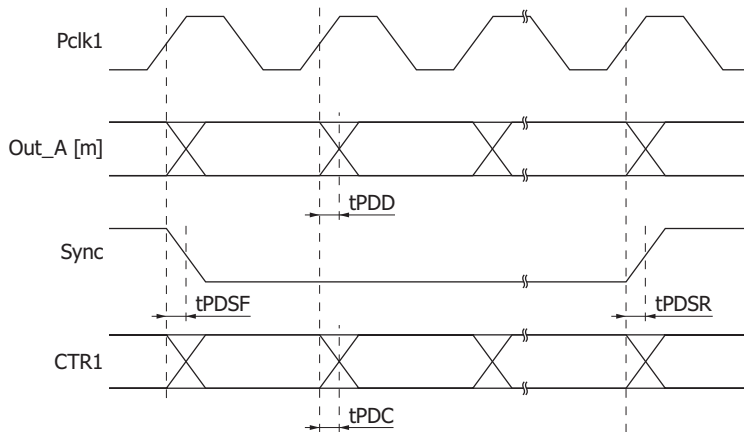*11: Pclk1_delay=0, Pclk3_delay=0
*12: CTR1_delay=0, CTR3_delay=0
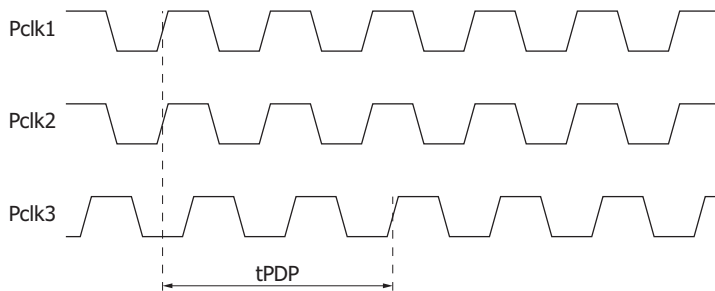
■ LVDS output voltage

KMPDC0658EB

■ Sync signal and video output

KMPDC0880EA

· Each waveform represents the difference between the LVDS positive signal and negative signal.
· Out_A[m] is video output of port A.
  m: 0=lower bit, 1=higher bit
· Video output starts after the rising of Sync. Sync can be used as reference of data acquisition [refer to Timing chart (P.12)].
· On the falling edge of CTR, the lower bits are output from D0 and the higher bits from D6. CTR can be used as reference of data acquisition [refer to Timing chart (P.12)].
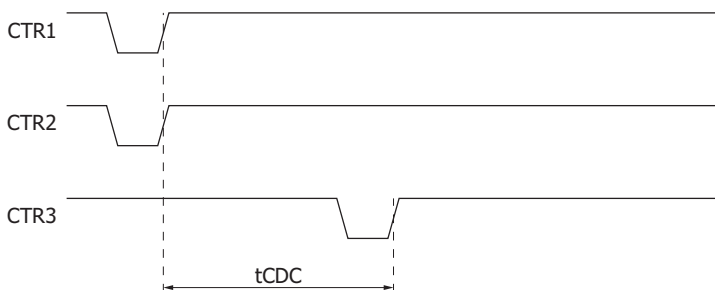
■ Bit output sync signals

KMPDC0889EA

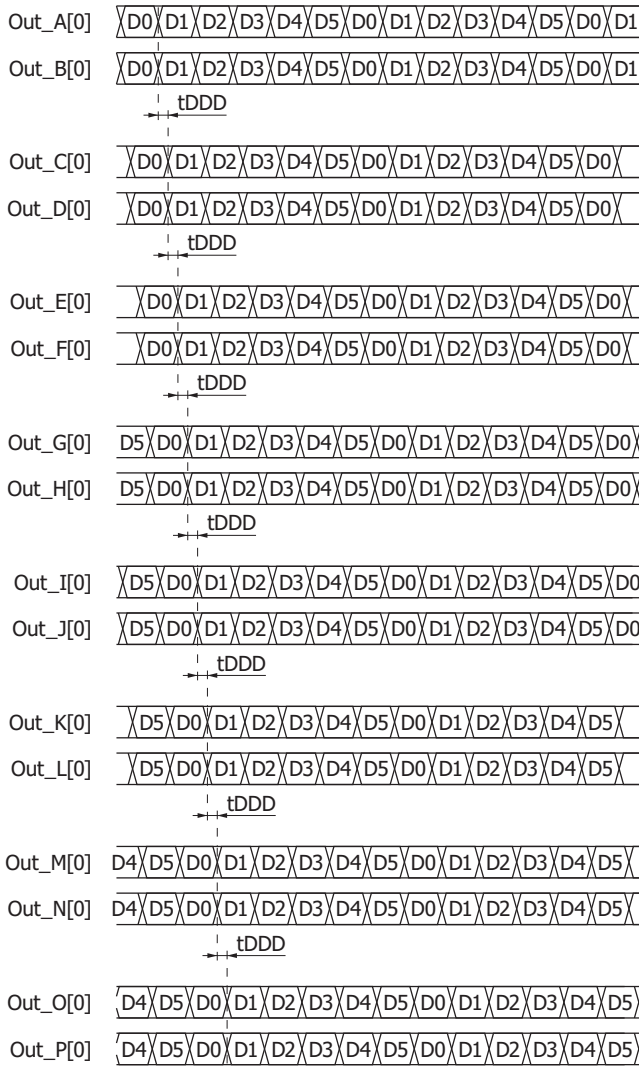Note: Timings are the same for Pclk1 and Pclk2 (setting: Pclk1_delay=0, Pclk2_delay=0).

■ Pixel output sync signals

KMPDC0890EA

Note: Timings are the same for CTR1 and CTR2 (setting: CTR1_delay=0, CTR2_delay=0).

■ Video output

| Out_A[0] | D0 D1 D2 D3 D4 D5 D0 D1 D2 D3 D4 D5 D0 D1 |
| Out_B[0] | D0 D1 D2 D3 D4 D5 D0 D1 D2 D3 D4 D5 D0 D1 |

tDDD

| Out_C[0] | D0 D1 D2 D3 D4 D5 D0 D1 D2 D3 D4 D5 D0 |
| Out_D[0] | D0 D1 D2 D3 D4 D5 D0 D1 D2 D3 D4 D5 D0 |

tDDD

| Out_E[0] | D0 D1 D2 D3 D4 D5 D0 D1 D2 D3 D4 D5 D0 |
| Out_F[0] | D0 D1 D2 D3 D4 D5 D0 D1 D2 D3 D4 D5 D0 |

tDDD

| Out_G[0] | D5 D0 D1 D2 D3 D4 D5 D0 D1 D2 D3 D4 D5 D0 |
| Out_H[0] | D5 D0 D1 D2 D3 D4 D5 D0 D1 D2 D3 D4 D5 D0 |

tDDD

| Out_I[0] | D5 D0 D1 D2 D3 D4 D5 D0 D1 D2 D3 D4 D5 D0 |
| Out_J[0] | D5 D0 D1 D2 D3 D4 D5 D0 D1 D2 D3 D4 D5 D0 |

tDDD

| Out_K[0] | D5 D0 D1 D2 D3 D4 D5 D0 D1 D2 D3 D4 D5 |
| Out_L[0] | D5 D0 D1 D2 D3 D4 D5 D0 D1 D2 D3 D4 D5 |

tDDD

| Out_M[0] | D4 D5 D0 D1 D2 D3 D4 D5 D0 D1 D2 D3 D4 D5 |
| Out_N[0] | D4 D5 D0 D1 D2 D3 D4 D5 D0 D1 D2 D3 D4 D5 |

tDDD

| Out_O[0] | D4 D5 D0 D1 D2 D3 D4 D5 D0 D1 D2 D3 D4 D5 |
| Out_P[0] | D4 D5 D0 D1 D2 D3 D4 D5 D0 D1 D2 D3 D4 D5 |

KMPDC0891EA

Note:
Timings are the same for each of the following.
· Port A to port B
· Port C to port D
· Port E to port F
· Port G to port H
· Port I to port J
· Port K to port L
· Port M to port N
· Port O to port P

Current consumption					
[Ta=25 °C, Vdd(A)=Vdd(D)=3.3 V, Vdd(C)=1.8 V, f(MCLK)=30 MHz, LR=100 klines/s]					
Parameter	Symbol	Min.	Typ.	Max.	Unit
Vdd(A) terminal[13]	Ic1	160	250	340	
Vdd(D) terminal[13]	Ic2	480	740	1000	mA
Vdd(C) terminal[13]	Ic3	440	680	920	

*13: Apply saturation exposure light.

▶ **Electrical characteristics of A/D converter [Ta=25 °C, Vdd(A)=Vdd(D)=3.3 V, Vdd(C)=1.8 V, f(MCLK)=30 MHz]**

Parameter		Symbol	Specification	Unit
Resolution	High-speed mode	RESO	10[14]	bit
	Low-speed mode		11[15]	
Conversion voltage range		-	0 to 1.3	V

*14: Equivalent to 10-bit. From offset output to saturated output is approximately 1024 DN.
*15: Equivalent to 11-bit. From offset output to saturated output is approximately 2048 DN.

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▣ Electrical and optical characteristics [Ta=25 °C, Vdd(A)=Vdd(D)=3.3 V, Vdd(C)=1.8 V, f(MCLK)=30 MHz, gain: default value, offset: default value, tpi(MST)=10 µs (high-speed mode), 20 µs (low-speed mode)]

Common to all modes						
Parameter		Symbol	Min.	Typ.	Max.	Unit
Spectral response range		λ		400 to 1000		nm
Peak sensitivity wavelength		λp	-	700	-	nm
Photoresponse nonuniformity[16]	Gain=1	PRNU	-	±5	±10	%
	Gain=8		-	±5	±10	
Image lag[17]	Gain=1	Lag	-	-	0.1	%
Saturation charge		Qsat	24	25	-	ke$^-$
SNR max.	Gain=1	-	42	44	-	dB
	Gain=8		32	35	-	

[16]: The output uniformity when a uniform light with a light exposure that is approximately 50% of saturation output is applied. It is defined as follows for the 8186 pixels excluding the 3 pixels at each end of the sensor.
PRNU = (ΔX/X) × 100 [%]

[17]: The signal component of the previous data that remains after data is read out under saturation output conditions. Image lag increases if light greater than the saturation exposure is incident.

High-speed mode						
Parameter	Symbol	Gain	Min.	Typ.	Max.	Unit
Offset variation[18]	VSNU	1	-	3.6	21.6	mV
			-	2.9	17.4	DN
		8	-	5.3	31.8	mV
			-	4.2	25.2	DN
Dark output[19]	VD	1	-	0.61	24	mV
			-	0.49	20	DN
		8	-	4.9	200	mV
			-	3.9	160	DN
Photosensitivity[20]	Sw	1	-	55	-	V/(lx·s)
			-	44k	-	DN/(lx·s)
		8	-	440	-	V/(lx·s)
			-	350k	-	DN/(lx·s)
Conversion efficiency	CE	1	-	51	-	µV/e$^-$
			-	41	-	mDN/e$^-$
		8	-	410	-	µV/e$^-$
			-	330	-	mDN/e$^-$
Saturation output	Vsat	-	1.2	1.25	-	V
			975	1000	-	DN
Readout noise[17]	Nread	1	-	0.63	3.4	mV-rms
			-	0.5	2.7	DN-rms
		8	-	1.5	16	mV-rms
			-	1.2	13	DN-rms
Dynamic range[18]	Drange	1	-	2000	-	-
		8	-	800	-	

Low-speed mode

Parameter	Symbol	Gain	Min.	Typ.	Max.	Unit
Offset variation[18]	VSNU	1	-	1.1	6.6	mV
			-	1.8	11	DN
		8	-	4.6	28	mV
			-	7.3	44	DN
Dark output[19]	VD	1	-	0.61	24	mV
			-	1	40	DN
		8	-	4.9	200	mV
			-	7.8	310	DN
Photosensitivity[20]	Sw	1	-	55	-	V/(lx·s)
			-	88k	-	DN/(lx·s)
		8	-	440	-	V/(lx·s)
			-	700k	-	DN/(lx·s)
Conversion efficiency	CE	1	-	51	-	μV/e$^-$
			-	82	-	mDN/e$^-$
		8	-	410	-	μV/e$^-$
			-	660	-	mDN/e$^-$
Saturation output	Vsat	-	1.2	1.25	-	V
			1950	2000	-	DN
Readout noise[21]	Nread	1	-	0.5	2.5	mV-rms
			-	0.76	3.8	DN-rms
		8	-	1.6	16	mV-rms
			-	2.5	26	DN-rms
Dynamic range[22]	Drange	1	-	2500	-	-
		8	-	800	-	

[18]: Measured in the dark state. Difference between the maximum and minimum.
[19]: Ts=10 ms, voltage difference from the offset output level
[20]: 2856 K, tungsten lamp
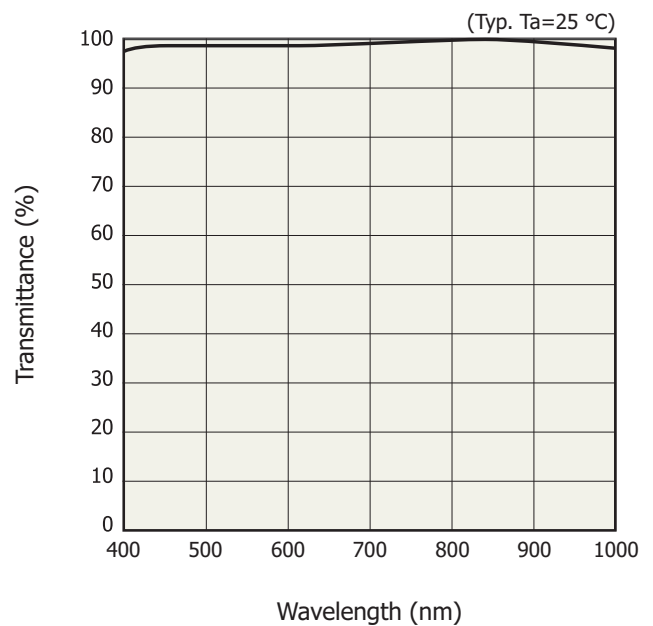[21]: Dark state
[22]: Vsat/Nread
Note: DN (digital number): unit of A/D converter output
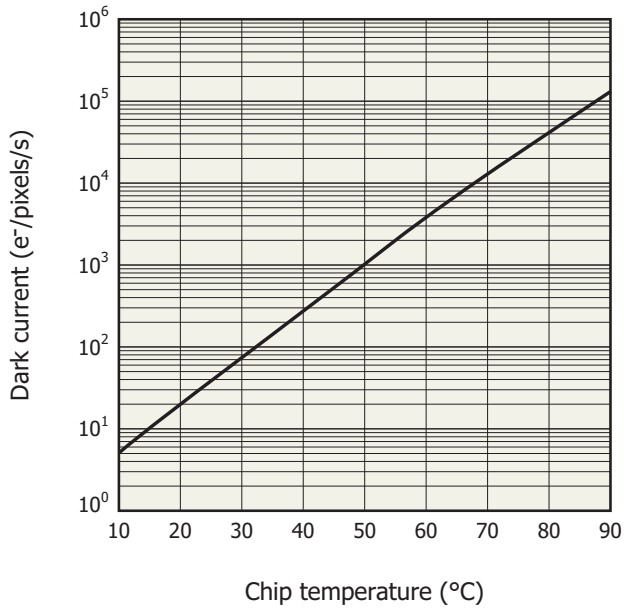
Spectral response (typical example)

(Ta=25 °C)

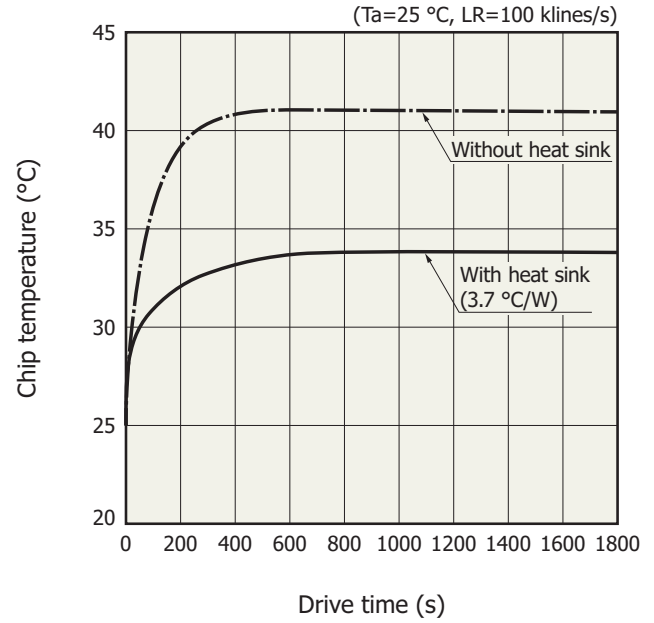

KMPDB0650EA

Spectral transmittance characteristics of window material

(Typ. Ta=25 °C)

KMPDB0494EA

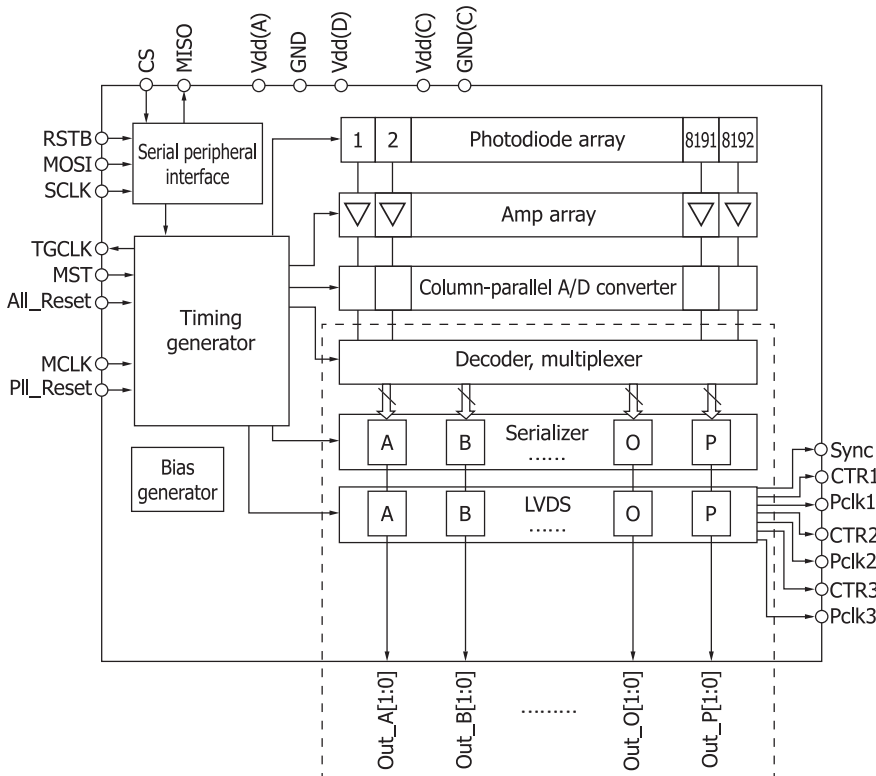## Dark current vs. chip temperature (typical example)

Chip temperature (°C)

KMPDB0618EA

Chip temperature vs. drive time (typical example)

(Ta=25 °C, LR=100 klines/s)

Drive time (s)

KMPDB0629EA

Note: Measures while keeping the ambient temperature steady in a constant temperature chamber.
If the ambient temperature rises, the chip temperature will rise. Take appropriate heat dissipation measures as required.
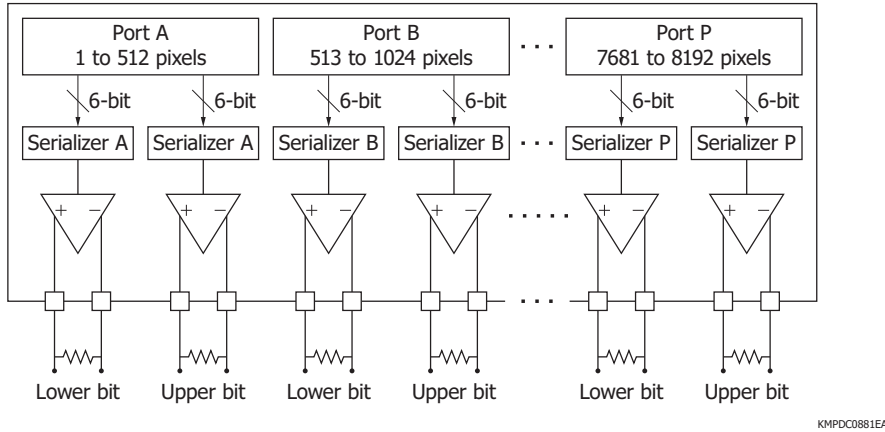
Block diagram

The video output signal is divided and output through 16 ports (A to P). Each port outputs 512 pixels of data (pixel numbers output from each port: A=1 to 512, B=513 to 1024, … P=7681 to 8192).

KMPDC0879EA
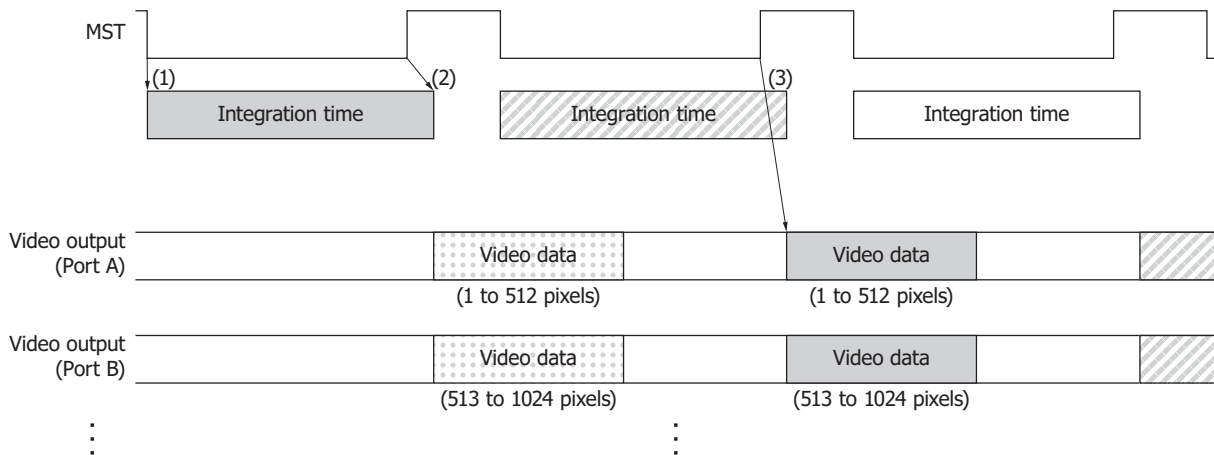
■ Enlarged view of video output (full output mode)

The output of each port is divided into upper and lower bit LVDS pairs.

KMPDC0881EA

Timing chart

■ Description of operation

The integration time is determined by the low period of the master start pulse.
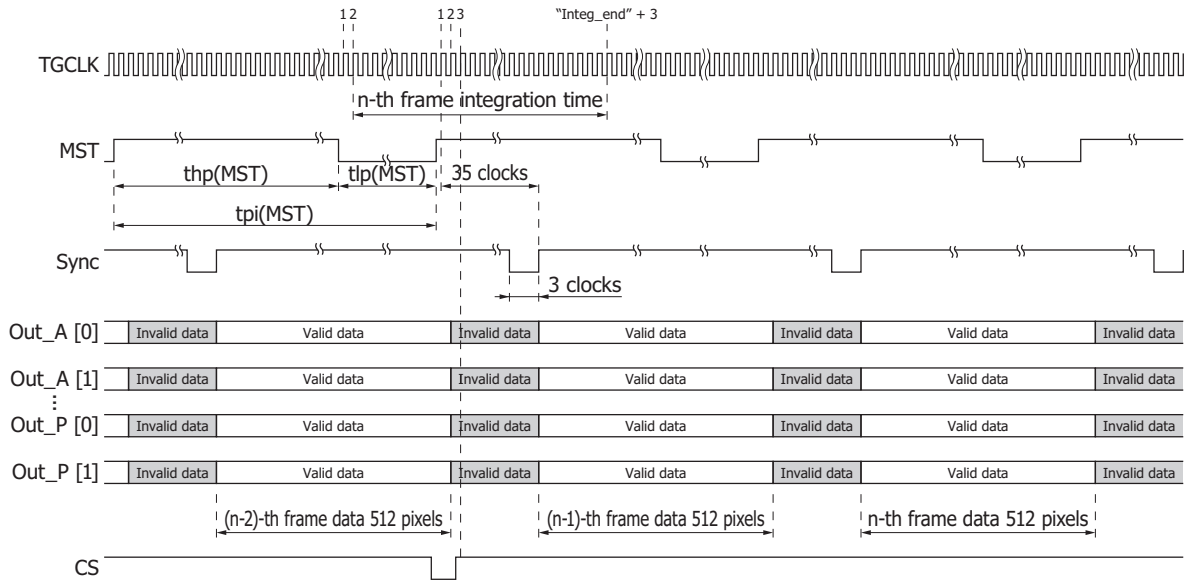

KMPDC0882EA

(1) The start of integration time is determined by the falling edge of the master start pulse.

(2) The end of integration time is determined by the rising edge of the master start pulse.

(3) Video data is output after the rising edge of the next master start pulse cycle. Video data is output in order from the first pixel.
    (512 pixels of data are output for each port.)

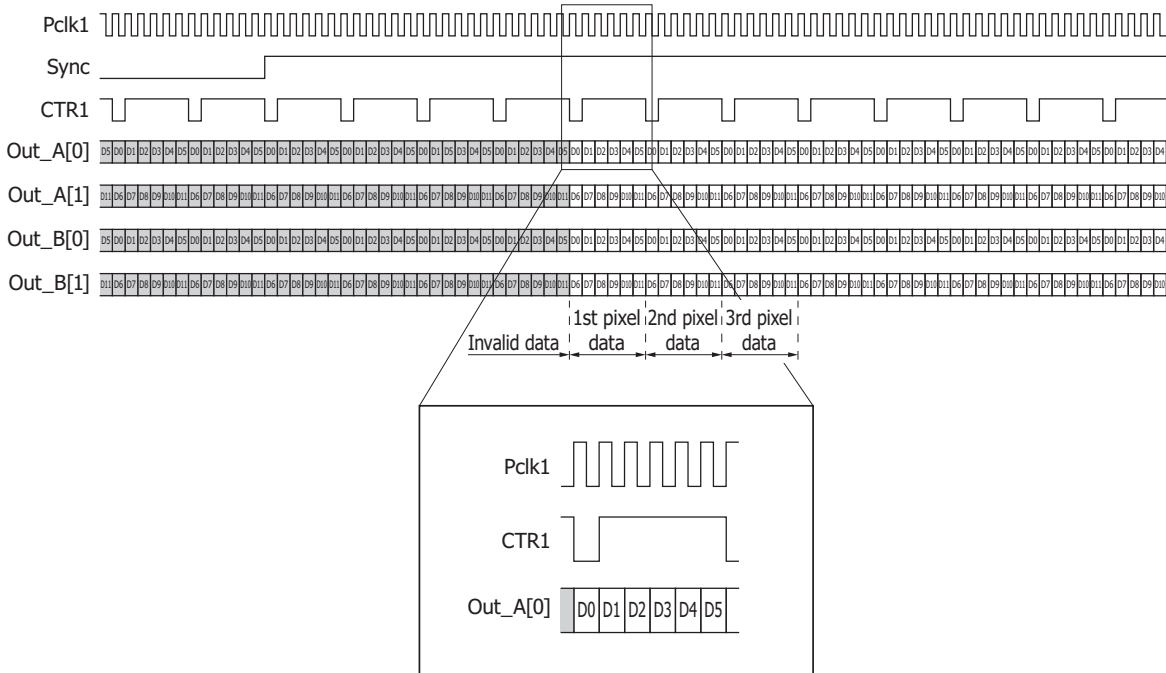* Signal integration is possible even during video output.

KMPDC0883EA

· Line rate equals the reciprocal of master start pulse cycle.
· TGCLK is a timing generator clock inside the sensor. TGCLK is the same frequency as that of MCLK in high-speed mode, and the 1/2 in low-speed mode.
· The integration time equals the low period of master start pulse plus "Integ_end" + 1 cycle of TGCLK.
· SPI set within 3 TGCLK clocks after the rising edge of the master start pulse is updated starting from the nth frame data.
· In 1/2 output mode, only the following outputs are valid.
  Out_A[0], Out_B[0], Out_C[0], Out_D[0], Out_E[0], Out_F[0], Out_G[0], Out_H[0]
  Out_I[0], Out_J[0], Out_K[0], Out_L[0], Out_M[0], Out_N[0], Out_O[0], Out_P[0]
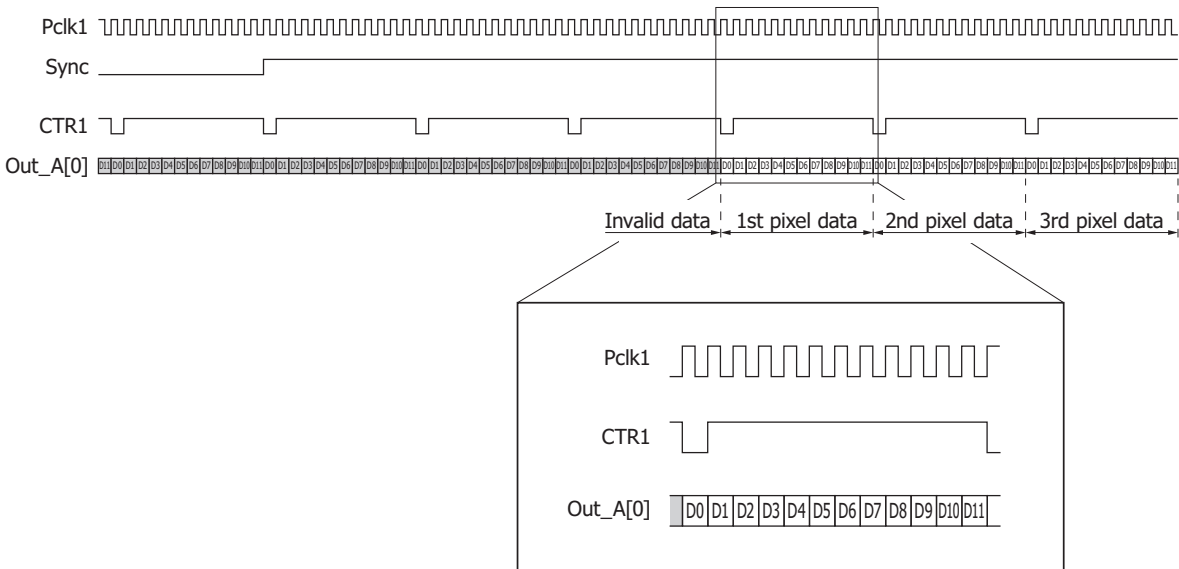
e.g., Port A, B

■ Full output mode (Pclk1_delay=0, CTR1_delay=0)

Pclk1

Sync

CTR1

Out_A[0]

Out_A[1]

Out_B[0]

Out_B[1]

Invalid data | 1st pixel data | 2nd pixel data | 3rd pixel data

Pclk1

CTR1

Out_A[0] D0 D1 D2 D3 D4 D5

KMPDC0884EB

■ 1/2 output mode (Pclk1_delay=0, CTR1_delay=0)

Pclk1

Sync

CTR1

Out_A[0]

Invalid data | 1st pixel data | 2nd pixel data | 3rd pixel data

Pclk1

CTR1

Out_A[0] D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11

KMPDC0885EB

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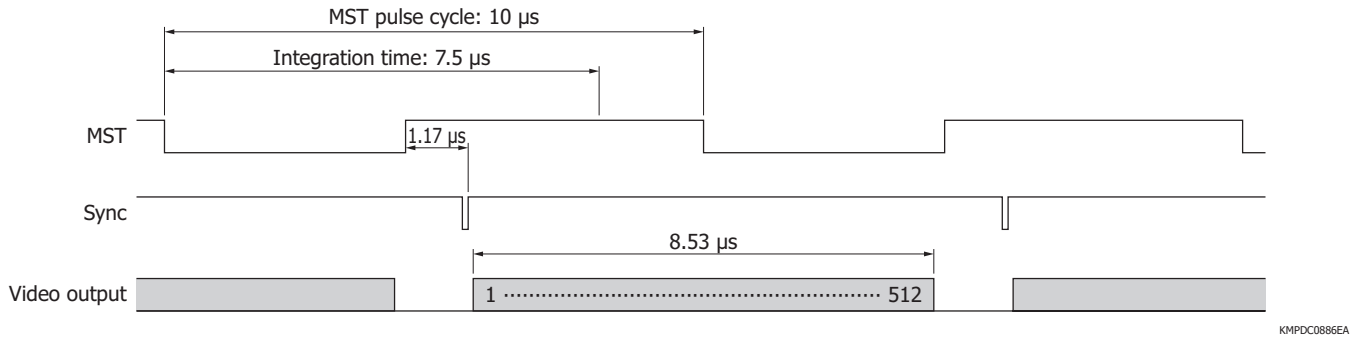## ▪ Operation examples

■ Example 1

Line rate=100 klines/s, master clock pulse frequency=30 MHz, high-speed mode, full output mode, integration time max., Integ_end=90
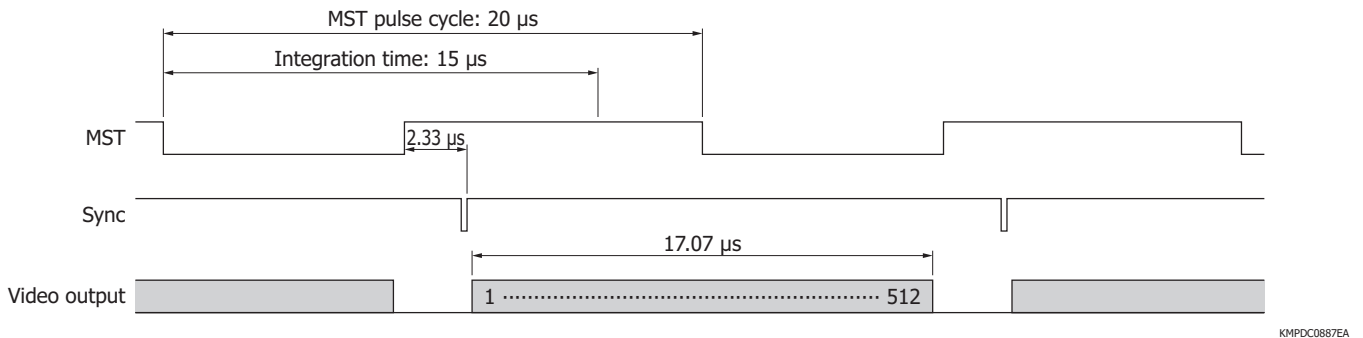

KMPDC0886EA

· Master start pulse cycle=300/f(MCLK)=10 μs (equals the reciprocal of start pulse cycle)
· Master start pulse's low period=Master start pulse cycle − High period min. of master start pulse

$\qquad$ =300/f(MCLK) - 166/f(MCLK)=300/30 MHz - 166/30 MHz=134/30 MHz=4.47 μs
· Integration time=Master start pulse's low period + (90 + 1) cycles of master clock pulses

$\qquad$ =(134 + 91)/30 MHz=7.5 μs

Sync rises approximately 1.17 μs after the rising edge of the master start pulse. Then the video output signal is output in order from the first pixel (512 pixels is output from each port).

■ Example 2

Line rate=50 klines/s, master clock pulse frequency=30 MHz, low-speed mode, 1/2 output mode, integration time max., Integ_end=90

KMPDC0887EA

· Master start pulse cycle=600/f(MCLK)=20 μs (equals the reciprocal of start pulse cycle)
· Master start pulse's low period=Master start pulse cycle − High period min. of master start pulse

$\qquad$ =600/f(MCLK) - 332/f(MCLK)=600/30 MHz - 332/30 MHz=268/30 MHz=8.93 μs
· Integration time=Master start pulse's low period + (90 + 1) × 2 cycles of master clock pulses

$\qquad$ =(268 + 182)/30 MHz=15 μs

Sync rises approximately 2.33 μs after the rising edge of the master start pulse. Then the video output signal is output in order from the first pixel (512 pixels is output from each port).

SPI address setting

Address (Decimal)	Register	Default value Binary	Default value Decimal	Setting	
0	Mode[1:0]	0	0	Mode[0]: high-speed/low-speed mode (default: high-speed mode) Mode[1]: number of video output (default: full output mode)	14
2	ADC_delay1[2:0]	- - - - -110	2	Drive timing of A/D converter, recommended setting=6	
13	ADC_delay2[4:0]	- - -0 1100	12	Drive timing of A/D converter, recommended setting=8	
14	Pclk1_delay[5:0]	- -00 0000	0	Pclk1 timing (default: Pclk1_delay[5:0]=0)	
15	CTR1_delay[5:0]	- -00 0000	0	CTR1 timing (default: CTR1_delay[5:0]=0)	
16	Pclk2_delay[5:0]	- -00 0000	0	Pclk2 timing (default: Pclk2_delay[5:0]=0)	
17	CTR2_delay[5:0]	- -00 0000	0	CTR2 timing (default: CTR2_delay[5:0]=0)	
18	Pclk3_delay[5:0]	- -00 0000	0	Pclk3 timing (default: Pclk3_delay[5:0]=0)	
19	CTR3_delay[5:0]	- -00 0000	0	CTR3 timing (default: CTR3_delay[5:0]=0)	
20	AGC[4:0]	- - -1 0000	16	Gain (default: gain=1)	
21	Offset[11:8]	- - - - 0000	31	Output offset (default: 31)	
22	Offset[7:0]	0001 1111			
23	ADC_delay3[3:0]	- - - - 0011	3	Drive timing of A/D converter, recommended setting=11	
26	ADC_delay4[7:0]	0000 0000	0	Drive timing of A/D converter, recommended setting=2	
43	ADC_delay5[5:0]	- -00 0000	0	Drive timing of A/D converter In the case of Mode[1]=0: recommended setting=0 In the case of Mode[1]=1: recommended setting=14	
51	Integ_end[7:0]	0110 1001	105	Setting when to end integration time (default: 105)	

Note: Always set the addresses shown in the above table. The image sensor may malfunction if any other address is set.

■ High-speed/low-speed mode

Maximum line rate is selectable from following 2 modes:
· High-speed mode (Mode[0]=0): Maximum line rate=100 klines/s, A/D converter resolution = 10-bit
                (From offset output to saturation output is approximately 1024 DN.)
· Low-speed mode (Mode[0]=1): Maximum line rate=50 klines/s, A/D converter resolution = 11-bit
                (From offset output to saturation output is approximately 2048 DN.)

■ Number of video output

The number of video output terminal is selectable from following 2 modes.
· Full output mode (Mode[1]=0): Video output=64 terminals (32 LVDS pairs)
· 1/2 output mode (Mode[1]=1): Video output=32 terminals (16 LVDS pairs)
  To make the line rate faster than 50 klines/s, do not use 1/2 output mode.

Note: Refer to the timing chart (P.12) in detail.

■ Drive timing of A/D converter

Use the recommended settings from the table above.

■ Pclk1, CTR1, Pclk2, CTR2, Pclk3, CTR3 timings

The output timings of Pclk1, CTR1, Pclk2, CTR2, Pclk3, and CTR3 can be delayed inside the sensor.
When the setting value is increased by 1, the output is delayed by approximately 0.15 ns.

■ Gain setting

The sensor may not operate properly if the settings are not shown in the table below. Use the settings in the table below.

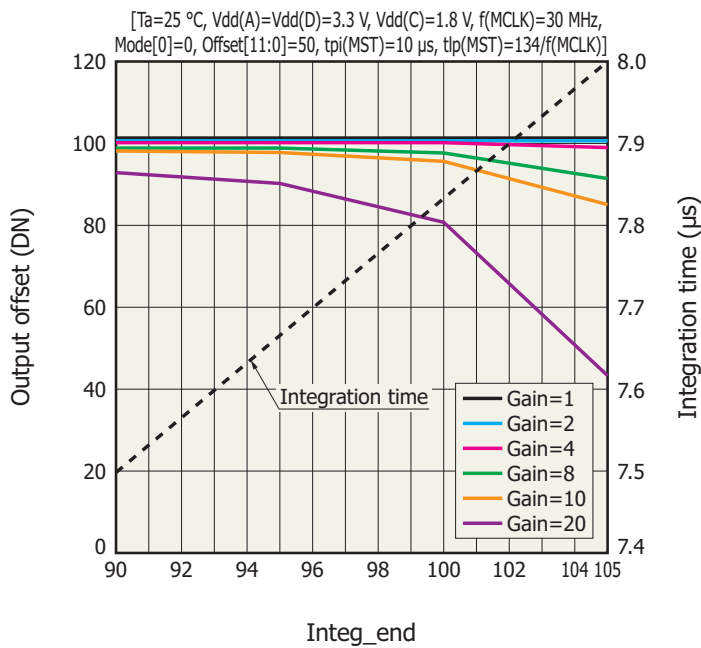| Decimal	AGC[4:0]					Gain	Description
	Binary						
	[4]	[3]	[2]	[1]	[0]		
0	0	0	0	0	0	20	
1	0	0	0	0	1	10	
2	0	0	0	1	0	8	
4	0	0	1	0	0	4	
8	0	1	0	0	0	2	
16	1	0	0	0	0	1	Default setting

■ Output offset setting

Set Offset[11:0] between 0 and 511. When Offset[11:0] is increased by 1, the offset value increases by 2 DN. Actual output offset value is set to be "Offset[11:0] × 2", but it will differ slightly as the gain of the amplifier increases because of chip variation, etc. Set offset[11:9] to 0.

■ Setting when to end integration time

Make settings so that "Integ_end[7: 0]=90 to 105." Timing of the integration time end will change depending on the setting value. By setting integration time to end earlier, it is possible to reduce offset fluctuation caused by gain settings.

▪ Output offset (average value of all pixels, typical example)

[Ta=25 °C, Vdd(A)=Vdd(D)=3.3 V, Vdd(C)=1.8 V, f(MCLK)=30 MHz, Mode[0]=0, Offset[11:0]=50, tpi(MST)=10 μs, tlp(MST)=134/f(MCLK)]
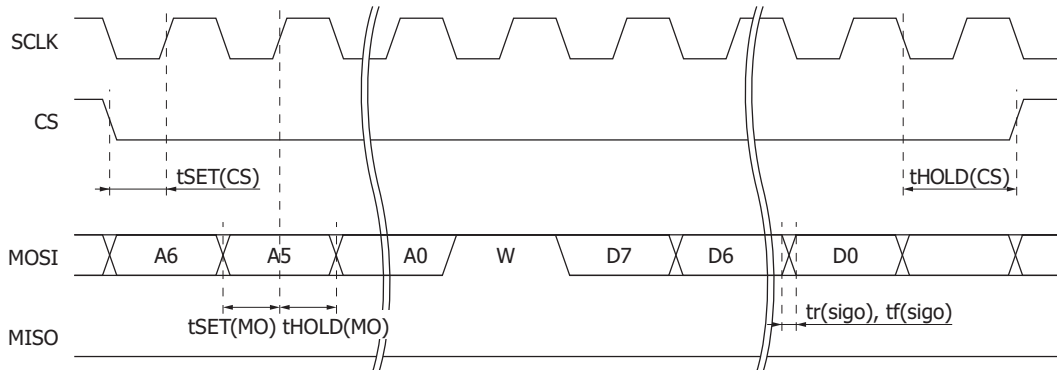
KMPDB0621EA

Note: For details, see the timing chart (P.11).

SPI setting

Set the SPI using SCLK, CS, and MOSI. Setting RSTB to low level resets all parameters (When setting RSTB, it is not necessary to consider RSTB pulse width or SCLK timing.).
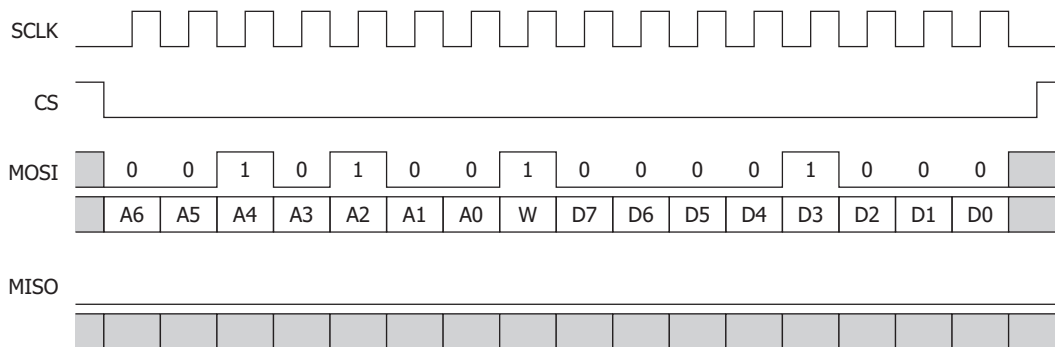

KMPDC0693EA

[Ta=25 °C, Vdd(A)=Vdd(D)=3.3 V, f(MCLK)=30 MHz, LR=100 klines/s]

Item	Symbol	Min.	Typ.	Max.	Unit
SPI clock pulse frequency	f(SCLK)	-	7.5	10	MHz
SPI setup time (CS)	tSET(CS)	7	-	-	ns
SPI hold time (CS)	tHOLD(CS)	7	-	-	ns
SPI setup time (MOSI)	tSET(MO)	7	-	-	ns
SPI hold time (MOSI)	tHOLD(MO)	7	-	-	ns
Digital input signal rise time[23]	tr(sigi)	-	5	7	ns
Digital input signal fall time[23]	tf(sigi)	-	5	7	ns

[23]: The time for input voltage to rise or fall between 10% and 90%
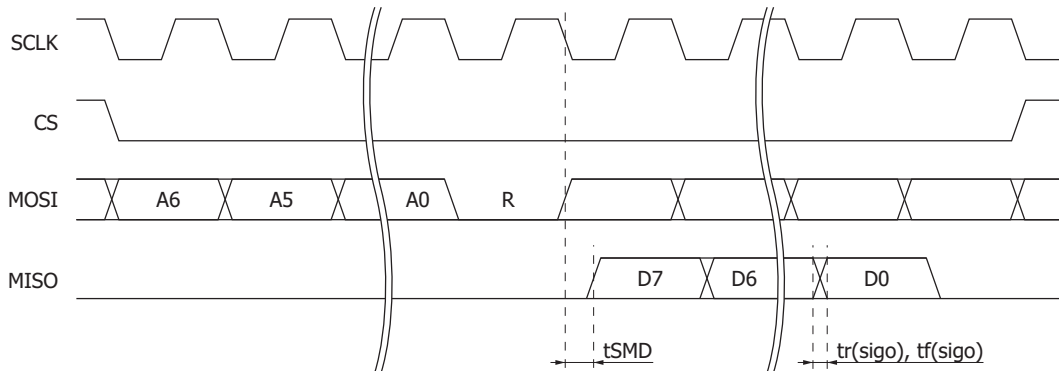
■ Example of SPI setting

Writing AGC[4:0]=8 (setting gain to 2 times)

KMPDC0694EA

Checking SPI setting

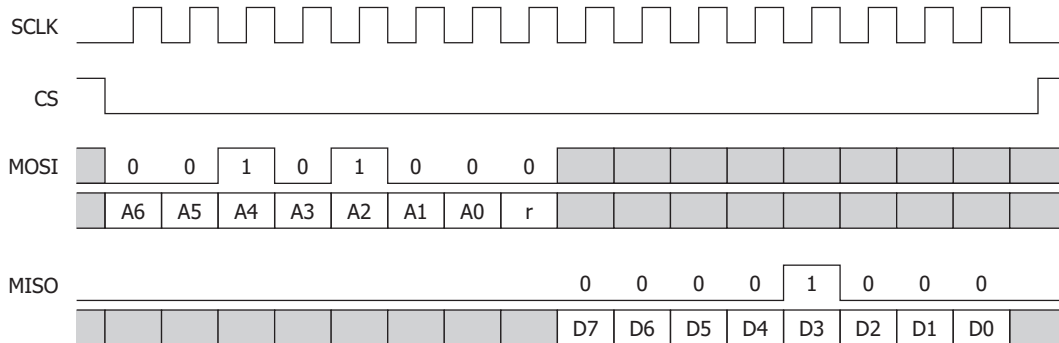You can check the current SPI setting in the following manner.

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[Ta=25 °C, Vdd(A)=Vdd(D)=3.3 V, f(MCLK)=30 MHz, LR=100 klines/s]

Item	Symbol	Min.	Typ.	Max.	Unit
Output signal rise time[24]	tr(sigo)	-	10	12	ns
Output signal fall time[24]	tf(sigo)	-	10	12	ns
Delay between SCLK and MISO	tSMD	-	-	25	ns

*24: Time for the output voltage to rise or fall between 10% and 90% when the load capacitance of the output terminal is 10 pF

■ Example of checking SPI setting

Confirm AGC[4:0]=8 (gain=twice)

KMPDC0696EA

Dimensional outline (unit: mm)

Tolerance unless otherwise noted: ±0.2
*1: Distance from FeNiCo alloy edge to photosensitive area last pixel (No.8192)
*2: Distance from FeNiCo alloy edge to photosensitive area center
*3: Distance from FeNiCo alloy surface to photosensitive surface
*4: Distance from FeNiCo alloy bottom to photosensitive surface
*5: Distance from FeNiCo alloy surface to glass surface
*6: Distance from glass surface to photosensitive surface
*7: Glass thickness
*8: FX23L-60S-0.5SV (HIROSE ELECTRIC)

KMPDA0363EA

Pin connections

■ Connector 1

Pin no.	Symbol	I/O	Function	Pin no.	Symbol	I/O	Function
V1	GND(C)	I	Ground	29	Out_Gp[1]	O	Video output signal (LVDS)
V2	Vdd(D)	I	Supply voltage (3.3 V)	30	Out_Gn[1]	O	Video output signal (LVDS)
V3	Vdd(C)	I	Supply voltage (1.8 V)	31	MST	I	Master start signal (single end)
V4	Vdd(D)	I	Supply voltage (3.3 V)	32	SCLK	I	SPI clock signal (single end)
1	MCLK	I	Master clock signal (single end)	33	MOSI	I	SPI input signal (single end)
2	TGCLK	O	Timing generator clock signal (single end)	34	MISO	O	SPI output signal (single end)
3	CS	I	SPI selection signal (single end)	35	PLL_Reset	I	PLL circuit reset (single end)
4	RSTB	I	SPI reset signal (single end)	36	All_Reset	I	Timing generator reset (single end)
5	Syncp	O	Frame sync signal (LVDS)	37	Pclk1p	O	Bit output sync signal (LVDS)
6	Syncn	O	Frame sync signal (LVDS)	38	Pclk1n	O	Bit output sync signal (LVDS)
7	Pclk2p	O	Bit output sync signal (LVDS)	39	CTR1p	O	Pixel sync signal (LVDS)
8	Pclk2n	O	Bit output sync signal (LVDS)	40	CTR1n	O	Pixel sync signal (LVDS)
9	CTR2p	O	Pixel sync signal (LVDS)	41	Out_Ap[0]	O	Video output signal (LVDS)
10	CTR2n	O	Pixel sync signal (LVDS)	42	Out_An[0]	O	Video output signal (LVDS)
11	Out_Ap[1]	O	Video output signal (LVDS)	43	GND	I	Ground
12	Out_An[1]	O	Video output signal (LVDS)	44	Out_Bp[0]	O	Video output signal (LVDS)
13	GND	I	Ground	45	Out_Bn[0]	O	Video output signal (LVDS)
14	Out_Bp[1]	O	Video output signal (LVDS)	46	GND	I	Ground
15	Out_Bn[1]	O	Video output signal (LVDS)	47	Out_Cp[0]	O	Video output signal (LVDS)
16	GND	I	Ground	48	Out_Cn[0]	O	Video output signal (LVDS)
17	Out_Cp[1]	O	Video output signal (LVDS)	49	GND	I	Ground
18	Out_Cn[1]	O	Video output signal (LVDS)	50	Out_Dp[0]	O	Video output signal (LVDS)
19	GND	I	Ground	51	Out_Dn[0]	O	Video output signal (LVDS)
20	Out_Dp[1]	O	Video output signal (LVDS)	52	GND	I	Ground
21	Out_Dn[1]	O	Video output signal (LVDS)	53	Out_Ep[0]	O	Video output signal (LVDS)
22	GND	I	Ground	54	Out_En[0]	O	Video output signal (LVDS)
23	Out_Ep[1]	O	Video output signal (LVDS)	55	GND	I	Ground
24	Out_En[1]	O	Video output signal (LVDS)	56	Out_Fp[0]	O	Video output signal (LVDS)
25	GND	I	Ground	57	Out_Fn[0]	O	Video output signal (LVDS)
26	Out_Fp[1]	O	Video output signal (LVDS)	58	GND	I	Ground
27	Out_Fn[1]	O	Video output signal (LVDS)	59	Out_Gp[0]	O	Video output signal (LVDS)
28	GND	I	Ground	60	Out_Gn[0]	O	Video output signal (LVDS)

■ Connector 2

Pin no.	Symbol	I/O	Function	Pin no.	Symbol	I/O	Function
V1	Vdd(A)	I	Supply voltage (3.3 V)	29	PCLK3p	O	Bit output sync signal (LVDS)
V2	GND(C)	I	Ground	30	PCLK3n	O	Bit output sync signal (LVDS)
V3	Vdd(A)	I	Supply voltage (3.3 V)	31	GND	I	Ground
V4	Vdd(C)	I	Supply voltage (1.8 V)	32	Out_Hp[0]	O	Video output signal (LVDS)
1	GND	I	Ground	33	Out_Hn[0]	O	Video output signal (LVDS)
2	Out_Hp[1]	O	Video output signal (LVDS)	34	GND	I	Ground
3	Out_Hn[1]	O	Video output signal (LVDS)	35	Out_Ip[0]	O	Video output signal (LVDS)
4	GND	I	Ground	36	Out_In[0]	O	Video output signal (LVDS)
5	Out_Ip[1]	O	Video output signal (LVDS)	37	GND	I	Ground
6	Out_In[1]	O	Video output signal (LVDS)	38	Out_Jp[0]	O	Video output signal (LVDS)
7	GND	I	Ground	39	Out_Jn[0]	O	Video output signal (LVDS)
8	Out_Jp[1]	O	Video output signal (LVDS)	40	GND	I	Ground
9	Out_Jn[1]	O	Video output signal (LVDS)	41	Out_Kp[0]	O	Video output signal (LVDS)
10	GND	I	Ground	42	Out_Kn[0]	O	Video output signal (LVDS)
11	Out_Kp[1]	O	Video output signal (LVDS)	43	GND	I	Ground
12	Out_Kn[1]	O	Video output signal (LVDS)	44	Out_Lp[0]	O	Video output signal (LVDS)
13	GND	I	Ground	45	Out_Ln[0]	O	Video output signal (LVDS)
14	Out_Lp[1]	O	Video output signal (LVDS)	46	GND	I	Ground
15	Out_Ln[1]	O	Video output signal (LVDS)	47	Out_Mp[0]	O	Video output signal (LVDS)
16	GND	I	Ground	48	Out_Mn[0]	O	Video output signal (LVDS)
17	Out_Mp[1]	O	Video output signal (LVDS)	49	GND	I	Ground
18	Out_Mn[1]	O	Video output signal (LVDS)	50	Out_Np[0]	O	Video output signal (LVDS)
19	GND	I	Ground	51	Out_Nn[0]	O	Video output signal (LVDS)
20	Out_Np[1]	O	Video output signal (LVDS)	52	GND	I	Ground
21	Out_Nn[1]	O	Video output signal (LVDS)	53	Out_Op[0]	O	Video output signal (LVDS)
22	GND	I	Ground	54	Out_On[0]	O	Video output signal (LVDS)
23	Out_Op[1]	O	Video output signal (LVDS)	55	GND	I	Ground
24	Out_On[1]	O	Video output signal (LVDS)	56	Out_Pp[0]	O	Video output signal (LVDS)
25	GND	I	Ground	57	Out_Pn[0]	O	Video output signal (LVDS)
26	Out_Pp[1]	O	Video output signal (LVDS)	58	GND	I	Ground
27	Out_Pn[1]	O	Video output signal (LVDS)	59	CTR3p	O	Pixel sync signal (LVDS)
28	GND	I	Ground	60	CTR3n	O	Pixel sync signal (LVDS)

Note: The video output symbol is defined as follows:

Out_An[0]

    [0]: lower (0 to 5) bits, [1]: higher (6 to 11) bits

    p: positive input of the differential pair, n: negative input of the differential pair

    A to P: output ports

Precautions

(1) Electrostatic countermeasures
This device has a built-in protection circuit against static electrical charges. However, to prevent destroying the device with electrostatic charges, take countermeasures such as grounding yourself, the workbench and tools. Also protect this device from surge voltages which might be caused by peripheral equipment.
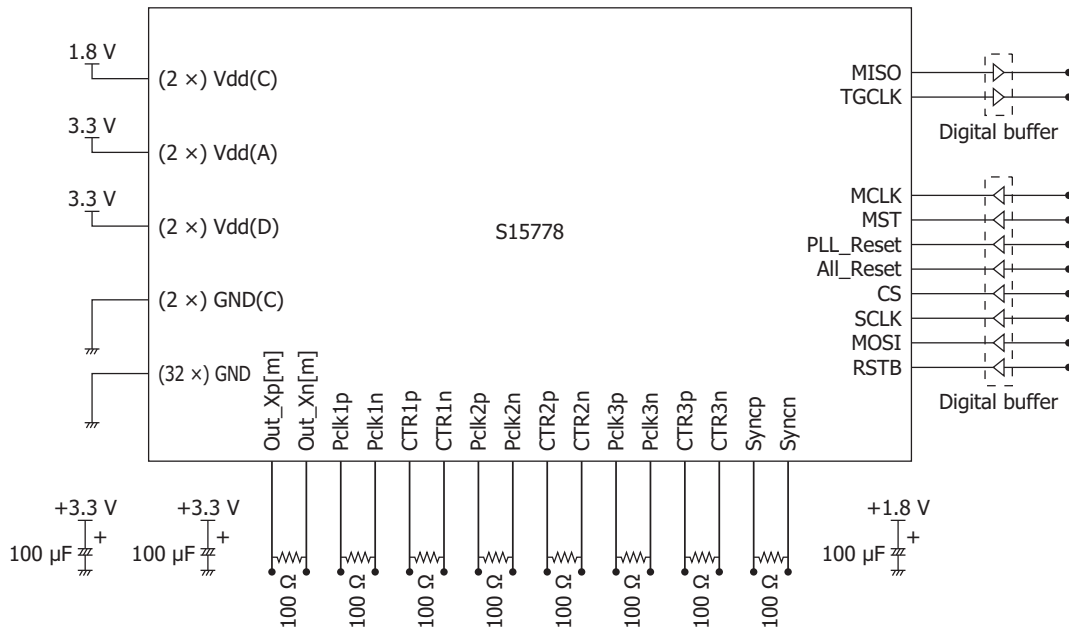
(2) Light input window
If dust or stain adheres to the surface of the light input window glass, it will appear as black spots on the image. When cleaning, avoid rubbing the window surface with dry cloth, dry cotton swab or the like, since doing so may generate static electricity. Use soft cloth, paper, a cotton swab, or the like moistened with alcohol to wipe off dust and stain. Then blow compressed air so that no stain remains.

(3) UV light irradiation
Because this product is not designed to resist characteristic deterioration under UV light irradiation, do not apply UV light irradiation to it.

Connection circuit example

Connect GND and GND(C) with a single point.
Digital buffer is not necessary if MISO or TGCLK is not used.

KMPDC0892EA

Related information

www.hamamatsu.com/sp/ssd/doc_en.html

■ Precautions
· Disclaimer
· Image sensors

Information described in this material is current as of April 2021.

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The product warranty is valid for one year after delivery and is limited to product repair or replacement for defects discovered and reported to us within that one year period. However, even if within the warranty period we accept absolutely no liability for any loss caused by natural disasters or improper product use. Copying or reprinting the contents described in this material in whole or in part is prohibited without our prior permission.