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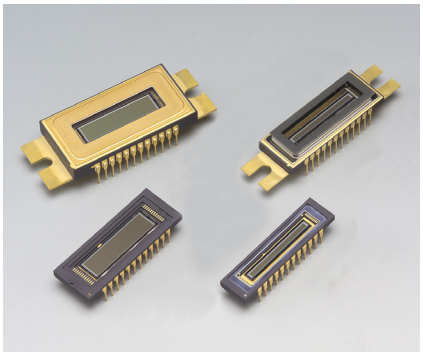
CCD area image sensor



S9972/S9973 series

Front-illuminated FFT-CCD, high near IR sensitivity

The S9972/S9973 series are families of FFT-CCD image sensors specifically designed for low-light-level detection in scientific applications. By using the binning operation, the S9972/S9973 series can be used as a linear image sensor having a long aperture in the direction of the device length. This makes the S9972/S9973 series ideally suited for use in spectrophotometry. The binning operation offers significant improvement in S/N and signal processing speed compared with conventional methods by which signals are digitally added by an external circuit. The S9972/S9973 series also feature low noise and low dark signal (MPP mode operation). This enables low-light-level detection and long integration time, thus achieving a wide dynamic range.
The S9972/S9973 series have an effective pixel size of 24 × 24 µm and are available in image areas of 24.576 (H) × 2.976 (V) mm^2 (1024 × 124 pixels) and 24.576 (H) × 6.048 (V) mm^2 (1024 × 252 pixels). The S9972/S9973 series are pin compatible with the S9970/S9971 series. (Operating conditions and characteristics are a little bit different from the S9970/S9971 series.)

Features

- **1024 (H) × 124 (V) and 1024 (H) × 252 (V) pixel format**
- **Pixel size: 24 × 24 µm**
- **Line/pixel binning**
- **100% fill factor**
- **Wide dynamic range**
- **Low dark signal**
- **Low readout noise**
- **MPP operation**
- **High near IR sensitivity**

Applications

- **Fluorescence spectrometer, ICP**
- **Raman spectrometer**
- **Industrial inspection requiring**
- **Semiconductor inspection**
- **DNA sequencer**
- **Low-light-level detection**

Selection guide

Type no.	Cooling	Number of total pixels	Number of active pixels	Active area [mm (H) × mm (V)]	Suitable multichannel detector head
S9972-1007	Non-cooled	1044 × 128	1024 × 124	24.576 × 2.976	C7020-02
S9972-1008		1044 × 256	1024 × 252	24.576 × 6.048	
S9973-1007	One-stage TE-cooled	1044 × 128	1024 × 124	24.576 × 2.976	C7021-02
S9973-1008		1044 × 256	1024 × 252	24.576 × 6.048	C7025-02

General ratings

Parameter	S9972-1007	S9972-1008	S9973-1007	S9973-1008
Pixel size	24 (H) × 24 (V) µm			
Vertical clock phase	2-phase			
Horizontal clock phase	2-phase			
Output circuit	One-stage MOSFET source follower			
Package	24-pin ceramic DIP (refer to dimensional outlines)			
Window*1	Quartz glass*2		Sapphire*3	AR-coated sapphire*3

*1: Temporary window type (ex. S9972-1007N) and UV coat type (ex. S9972-1007UV) are available upon request.
(On the temporary window type, a window is temporarily attached by tape to protect the CCD chip and wires.)
*2: Resin sealing
*3: Hermetic sealing

Absolute maximum ratings (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating temperature	Topr	-50	-	+50	°C
Storage temperature	Tstg	-50	-	+70	°C
Output transistor drain voltage	V_{OD}	-0.5	-	+25	V
Reset drain voltage	V_{RD}	-0.5	-	+18	V
Test point (vertical input source)	V_{ISV}	-0.5	-	+18	V
Test point (horizontal input source)	V_{ISH}	-0.5	-	+18	V
Test point (vertical input gate)	V_{IG1V}, V_{IG2V}	-15	-	+15	V
Test point (horizontal input gate)	V_{IG1H}, V_{IG2H}	-15	-	+15	V
Summing gate voltage	V_{SG}	-15	-	+15	V
Output gate voltage	V_{OG}	-15	-	+15	V
Reset gate voltage	V_{RG}	-15	-	+15	V
Transfer gate voltage	V_{TG}	-15	-	+15	V
Vertical shift register clock voltage	V_{P1V}, V_{P2V}	-15	-	+15	V
Horizontal shift register clock voltage	V_{P1H}, V_{P2H}	-15	-	+15	V

Operating conditions (MPP mode, Ta=25 °C)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Output transistor drain voltage		V_{OD}	18	20	22	V
Reset drain voltage		V_{RD}	12	13	14	V
Output gate voltage		V_{OG}	-0.5	0	2	V
Substrate voltage		V_{SS}	-	0	-	V
Test point (vertical input source)		V_{ISV}	-	V_{RD}	-	V
Test point (horizontal input source)		V_{ISH}	-	V_{RD}	-	V
Test point (vertical input gate)		V_{IG1V}, V_{IG2V}	-8	0	-	V
Test point (horizontal input gate)		V_{IG1H}, V_{IG2H}	-8	0	-	V
Vertical shift register clock voltage	High	V_{P1VH}, V_{P2VH}	0	4	6	V
	Low	V_{P1VL}, V_{P2VL}	-9	-8	-7	
Horizontal shift register clock voltage	High	V_{P1HH}, V_{P2HH}	0	4	6	V
	Low	V_{P1HL}, V_{P2HL}	-9	-8	-7	
Summing gate voltage	High	V_{SGH}	0	4	6	V
	Low	V_{SGL}	-9	-8	-7	
Reset gate voltage	High	V_{RGH}	0	4	6	V
	Low	V_{RGL}	-9	-8	-7	
Transfer gate voltage	High	V_{TGH}	0	4	6	V
	Low	V_{TGL}	-9	-8	-7	
External load resistance		R_L	9	10	11	kΩ

Electrical characteristics (Ta=25 °C)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Signal output frequency		fc	-	0.1	1	MHz
Vertical shift register capacitance	S9972/S9973-1007	C_{P1V}, C_{P2V}	-	1600	-	pF
	S9972/S9973-1008		-	3200	-	
Horizontal shift register capacitance		C_{P1H}, C_{P2H}	-	180	-	pF
Summing gate capacitance		C_{SG}	-	7	-	pF
Reset gate capacitance		C_{RG}	-	7	-	pF
Transfer gate capacitance		C_{TG}	-	100	-	pF
Transfer efficiency*4		CTE	0.99995	0.99999	-	-
DC output level		Vout	12	15	18	V
Output impedance		Zo	-	3	-	kΩ
Power dissipation*5		P	-	15	-	mW

*4: Charge transfer efficiency per pixel, measured at half of the full well capacity
*5: Power dissipation of the on-chip amplifier plus load resistance

Electrical and optical characteristics (Ta=25 °C, unless otherwise noted)

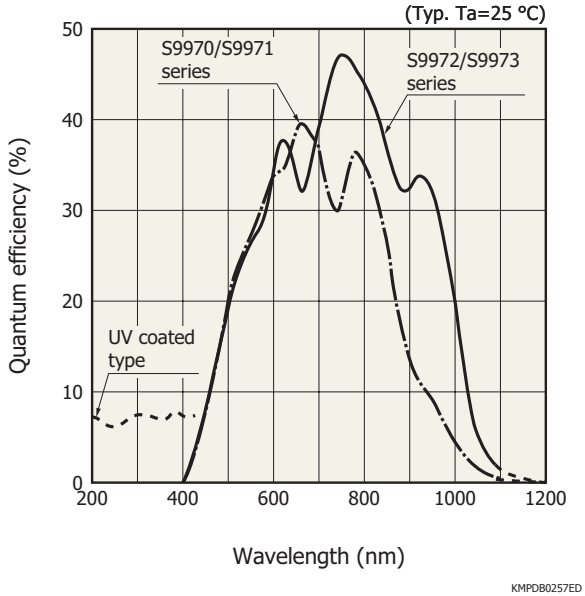
Parameter		Symbol	Min.	Typ.	Max.	Unit
Saturation output voltage		Vsat	-	Fw × CE	-	V
Full well capacity	Vertical	Fw	120	240	-	ke⁻
	Horizontal		240	480	-	
Conversion efficiency*6		CE	-	2.8	-	μV/e⁻
Dark current*7 (MPP mode)	+25 °C	DS	-	2000	30000	e⁻/pixel/s
	0 °C		-	100	1500	
Readout noise*8		Nread	-	4	18	e⁻rms
Dynamic range*9	Line binning	Drange	60000	120000	-	-
	Area scanning		30000	60000	-	
Spectral response range		λ	-	400 to 1100	-	nm
Photo response non-uniformity*10		PRNU	-	-	±10	%
Blemish	Point defects*11	-	-	-	0	-
	Cluster defects*12		-	-	0	
	Column defects*13		-	-	0	

*6: V_{OD}=20 V , Load resistance=10 kΩ
*7: Dark current nearly doubles for every 5 to 7 °C increase in temperature.
*8: Operating frequency 80 kHz, temperature -40 °C
*9: Dynamic range = Full well capacity / Readout noise
*10: Measured at one-half of the saturation output (full well capacity) using LED light (peak emission wavelength: 560 nm)

$$\text{Photo response non-uniformity} = \frac{\text{Fixed pattern noise (peak to peak)}}{\text{Signal}} \times 100\ [\%]$$

*11: White spots
Pixels that generate dark current higher than 3% of the saturation. (Measured at 0 °C, Ts=1 s)
Black spots
Pixels whose sensitivity is lower than one-half of the average pixel output (Measured with uniform light producing one-half of the saturation charge)
*12: 2 to 9 consecutive image defects
*13: 10 or more consecutive image defects

Spectral response (without window)*14



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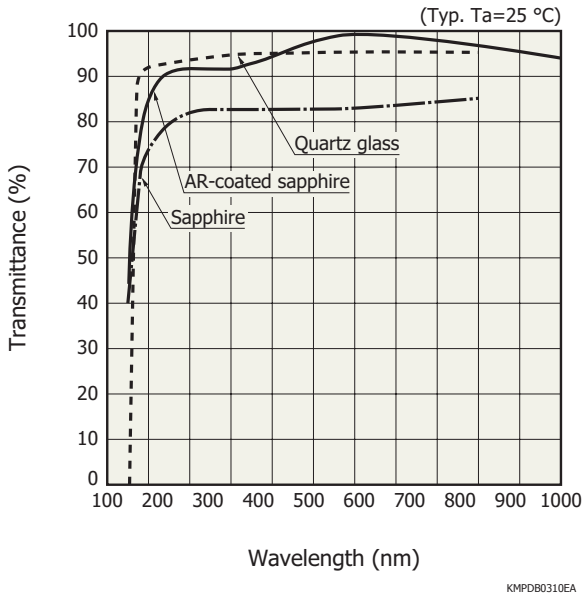
Spectral transmittance characteristics



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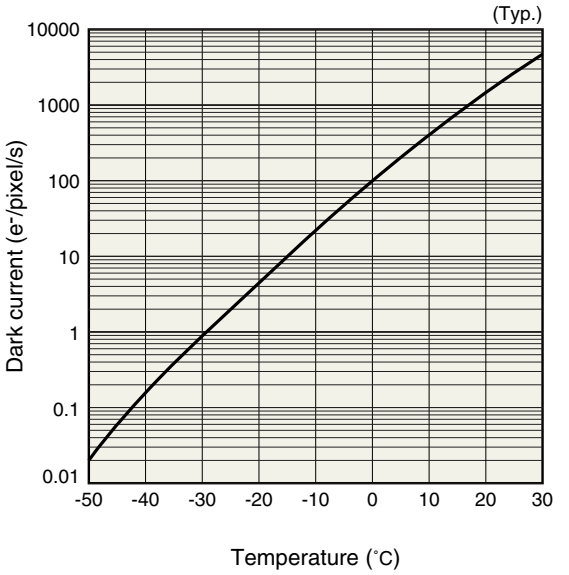
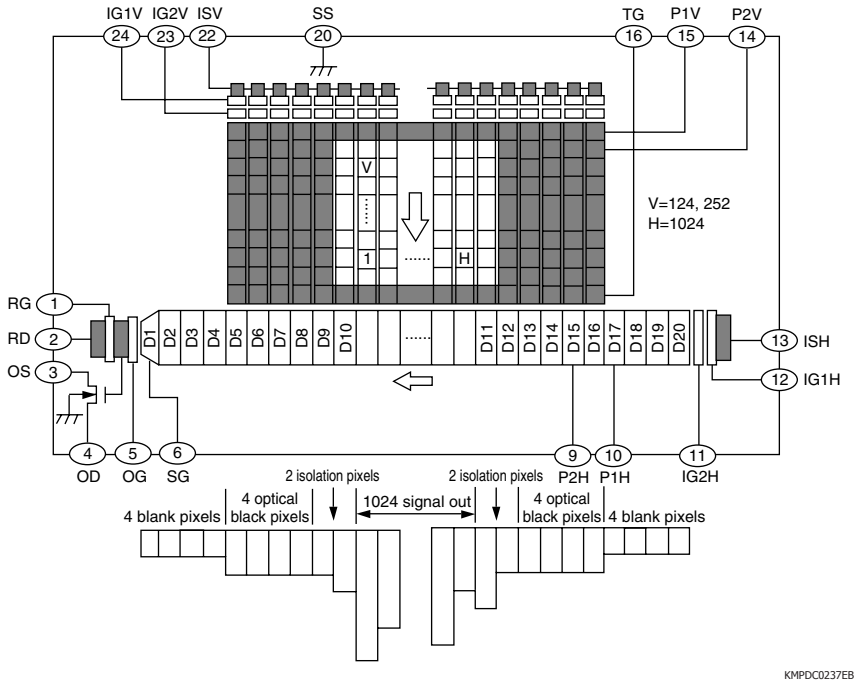
*14: Spectral response with sapphire or AR-coated sapphire is decreased according to the spectral transmittance characteristic of window material.

Dark current vs. temperature



Device structure (schematic as viewed from top of dimensional outlines)



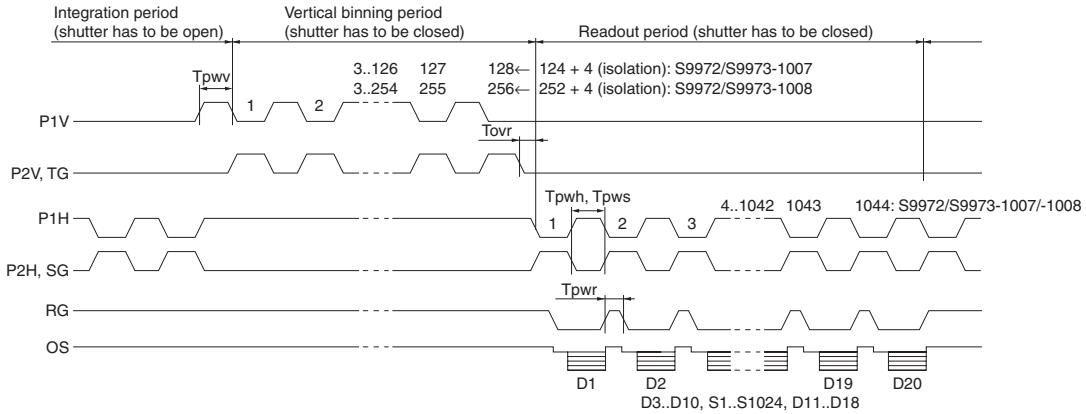
Pixel format

Left ← Horizontal Direction → Right						
Blank	Optical Black	Isolation	Effective	Isolation	Optical Black	Blank
4	4	2	1024	2	4	4

Top ← Vertical Direction → Bottom		
Isolation	Effective	Isolation
2	124 or 252	2

Timing chart

Line binning



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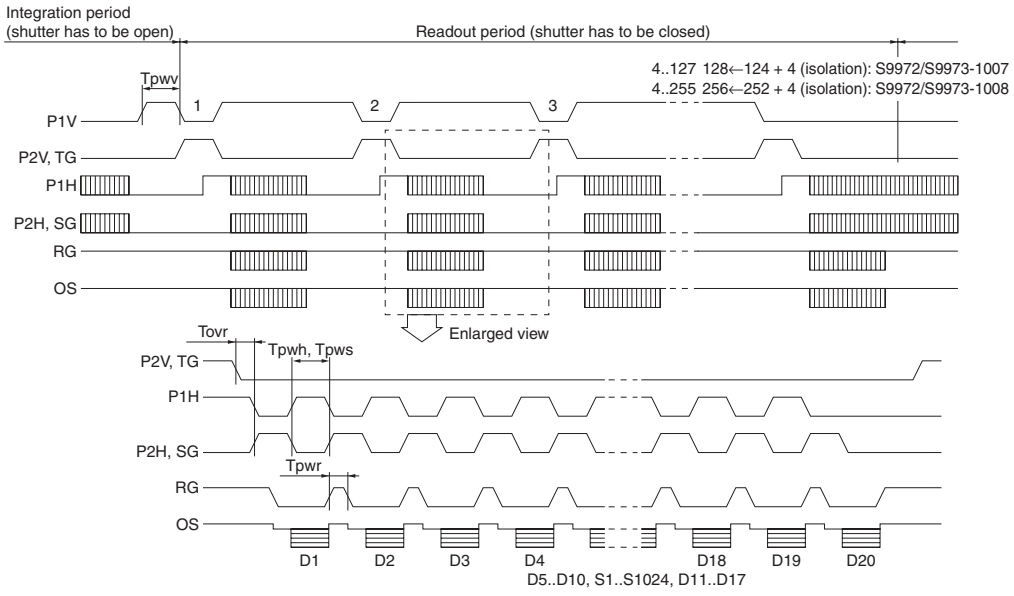
Area scanning (large full well mode)



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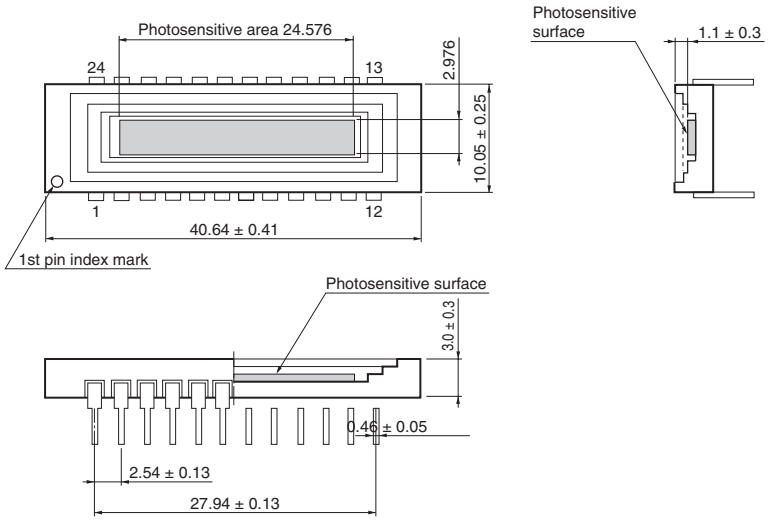
Parameter			Symbol	Min.	Typ.	Max.	Unit
P1V, P2V, TG	Pulse width*15	S9972/S9973-1007	Tpwv	6.0	18	-	µs
		S9972/S9973-1008		12	36	-	
	Rise and fall times		Tprv, Tpfv	200	-	-	ns
P1H, P2H	Pulse width		Tpwh	500	5000	-	ns
	Rise and fall times*15		Tprh, Tpfh	10	-	-	ns
	Duty ratio		-	-	50	-	%
SG	Pulse width		Tpws	500	5000	-	ns
	Rise and fall times		Tprs, Tpfs	10	-	-	ns
	Duty ratio		-	-	50	-	%
RG	Pulse width		Tpwr	100	500	-	ns
	Rise and fall times		Tprr, Tpfr	5	-	-	ns
TG - P1H	Overlap time		Tovr	3	6	-	µs

*15: Symmetrical clock pulses should be overlapped at 50% of maximum amplitude.

Dimensional outlines (unit: mm)

S9972-1007



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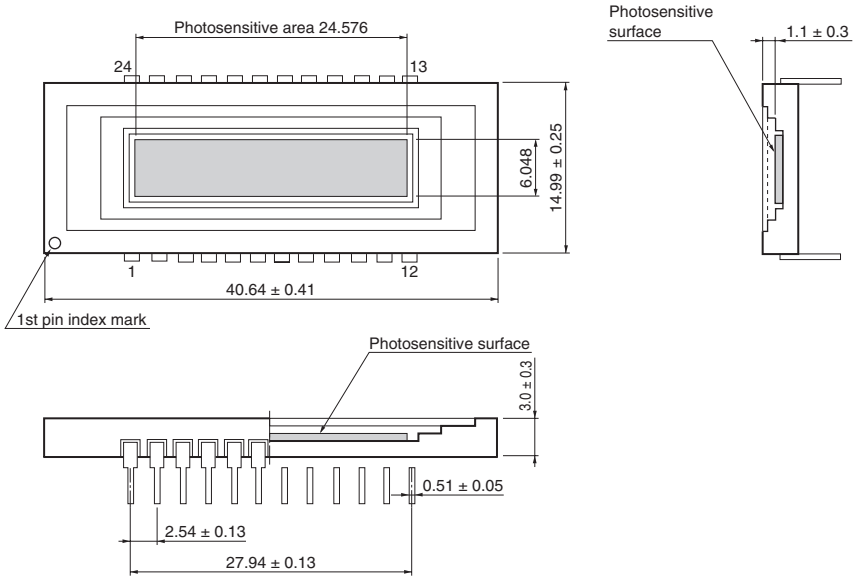
S9972-1008



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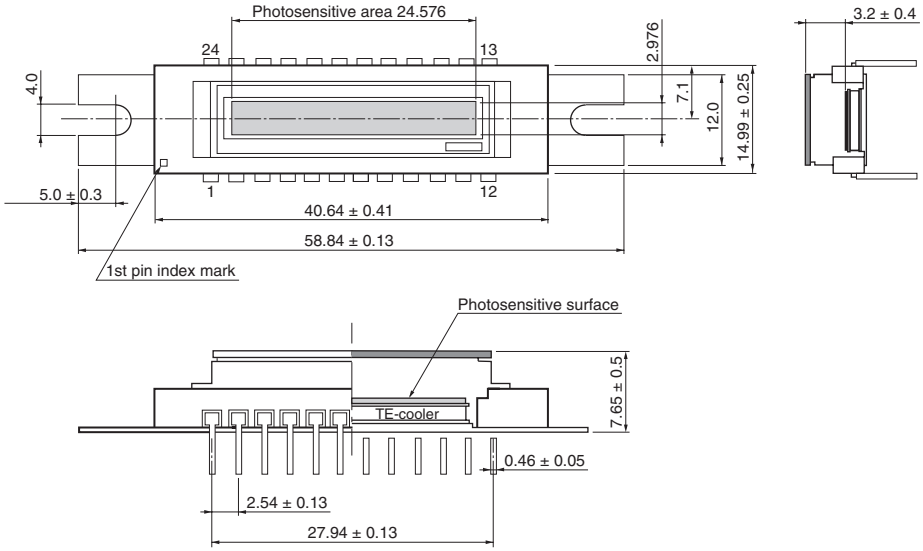
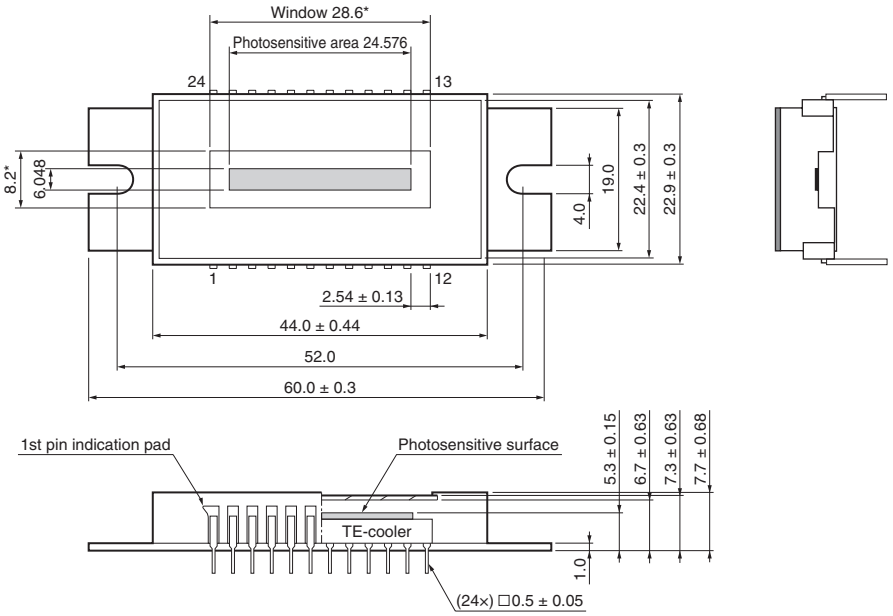
S9973-1007



KMPDA0206EC

S9973-1008



* Size of window that guarantees the transmittance in the "Spectral transmittance characteristics of window material" graph

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Pin connections

Pin No.	S9972 series		S9973 series		Remark (standard operation)
	Symbol	Description	Symbol	Description	
1	RG	Reset gate	RG	Reset gate	
2	RD	Reset drain	RD	Reset drain	+13 V
3	OS	Output transistor source	OS	Output transistor source	R_L=10 kΩ
4	OD	Output transistor drain	OD	Output transistor drain	+20 V
5	OG	Output gate	OG	Output gate	0 V
6	SG	Summing gate	SG	Summing gate	Same timing as P2H
7	-		Th1	Thermistor	
8	-		Th2	Thermistor	
9	P2H	CCD horizontal register clock-2	P2H	CCD horizontal register clock-2	
10	P1H	CCD horizontal register clock-1	P1H	CCD horizontal register clock-1	
11	IG2H	Test point (horizontal input gate-2)	IG2H	Test point (horizontal input gate-2)	0 V
12	IG1H	Test point (horizontal input gate-1)	IG1H	Test point (horizontal input gate-1)	0 V
13	ISH	Test point (horizontal input source)	ISH	Test point (horizontal input source)	Shorted to RD
14	P2V	CCD vertical register clock-2	P2V	CCD vertical register clock-2	
15	P1V	CCD vertical register clock-1	P1V	CCD vertical register clock-1	
16	TG*16	Transfer gate	TG*16	Transfer gate	Same timing as P2V
17	-		-		
18	-		P-	TE-cooler-	
19	-		P+	TE-cooler+	
20	SS	Substrate (GND)	SS	Substrate (GND)	GND
21	-		-		
22	ISV	Test point (vertical input source)	ISV	Test point (vertical input source)	Shorted to RD
23	IG2V	Test point (vertical input gate-2)	IG2V	Test point (vertical input gate-2)	0 V
24	IG1V	Test point (vertical input gate-1)	IG1V	Test point (vertical input gate-1)	0 V

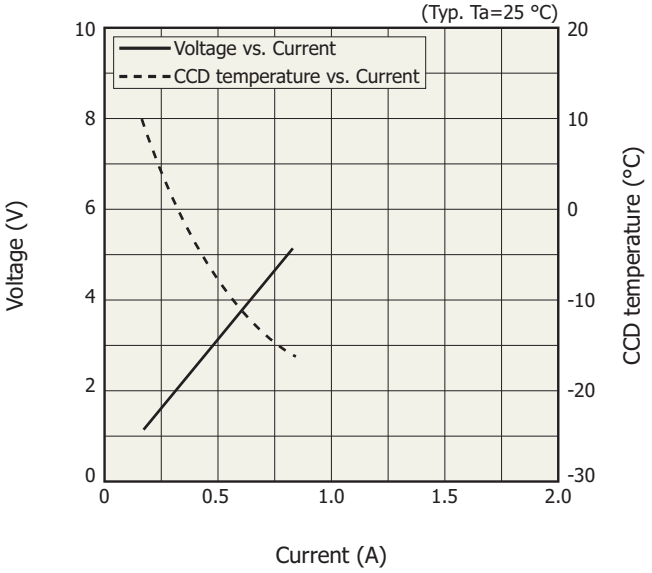
*16: Isolation gate between vertical register and horizontal register. In standard operation, TG should be applied the same pulse as P2V.

Specifications of built-in TE-cooler (Typ.)

Parameter	Symbol	Condition	S9973-1007	S9973-1008	Unit
Internal resistance	Rint	Ta=25 °C	6.0	1.2	Ω
Maximum current*17	Imax	Tc*18=Th*19=25 °C	1.5	3.0	A
Maximum voltage	Vmax	Tc*18=Th*19=25 °C	8.8	3.6	V
Maximum heat absorption*20	Qmax		6.7	5.1	W
Maximum temperature of hot side	-		70		°C

*17: If the current is greater than Imax, the heat absorption begins to decrease due to the Joule heat. It should be noted that this value is not a damage threshold. To protect the thermoelectric cooler and maintain stable operation, the supply current should be less than 60 % of this maximum current.
*18: Temperature of cool side of thermoelectric cooler
*19: Temperature of hot side of thermoelectric cooler
*20: This is a heat absorption when the maximum current is supplied to the TE-cooler.

S9973-1007



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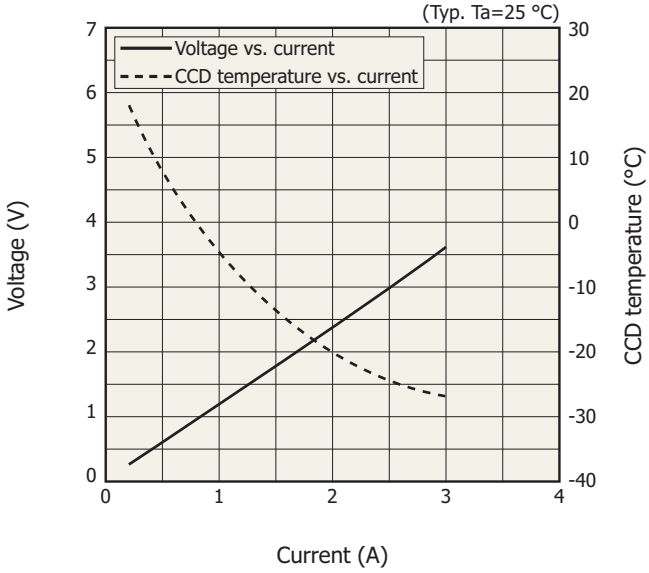
S9973-1008



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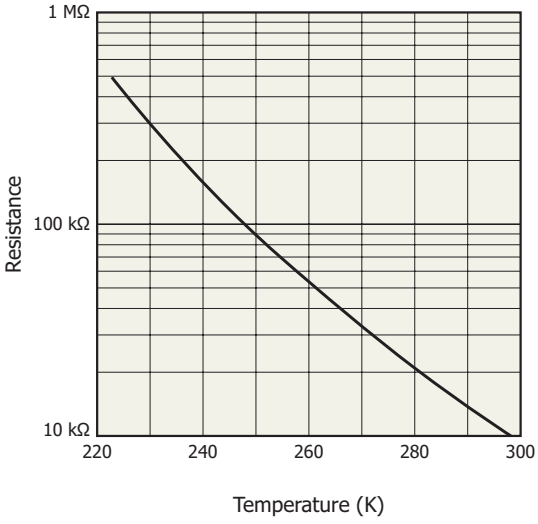
Specifications of built-in temperature sensor

A thermistor chip is built into the same package with a CCD chip and monitors the operating CCD chip temperature.
The relation between this thermistor's resistance and absolute temperature is express by the following equation.

$R_{T1} = R_{T2} \times \exp B_{T1/T2} (1/T1 - 1/T2)$

R_{T1}: resistance at absolute temperature T1 [K]
R_{T2}: resistance at absolute temperature T2 [K]
$B_{T1/T2}$: B constant [K]

The characteristics of the thermistor used are as follows.
R_{298}=10 kΩ
$B_{298/323}$=3450 K



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Precautions (electrostatic countermeasures)

· Handle these sensors with bare hands or wearing cotton gloves. In addition, wear anti-static clothing or use a wrist band with an earth ring, in order to prevent electrostatic damage due to electrical charges from friction.
· Do not place the sensor directly on workbenches or floors that may become charged with static electricity.
· Connect a ground wire to workbenches or floors in order to discharge static electricity.
· Ground tools, such as tweezers and soldering irons, that are used to handle the sensor.

It is not always necessary to provide all the electrostatic countermeasures stated above. Implement these countermeasures according to the extent of deterioration or damage that may occur.

Temperature gradient rate for cooling or heating of element

When using an external cooler, set the temperature gradient rate for cooling or heating the element to 5 K/minute or less.

Related information

www.hamamatsu.com/sp/ssd/doc_en.html

■ Precautions
· Disclaimer
· Image sensors

■ Technical information
· FFT-CCD area image sensor/Technical information
· Image sensors/Terminology

Multichannel detector head (C7020-02, C7021-02, C7025-02)

Features

- **C7020-02: for S9972 series**
  C7021-02: for S9973-1007
  C7025-02: for S9973-1008
- **Area scanning or full line-binnng operation**
- **Readout frequency: 250 kHz**
- **Readout noise: 20 e⁻rms**
- **ΔT=50 °C (ΔT changes by radiation method.)**

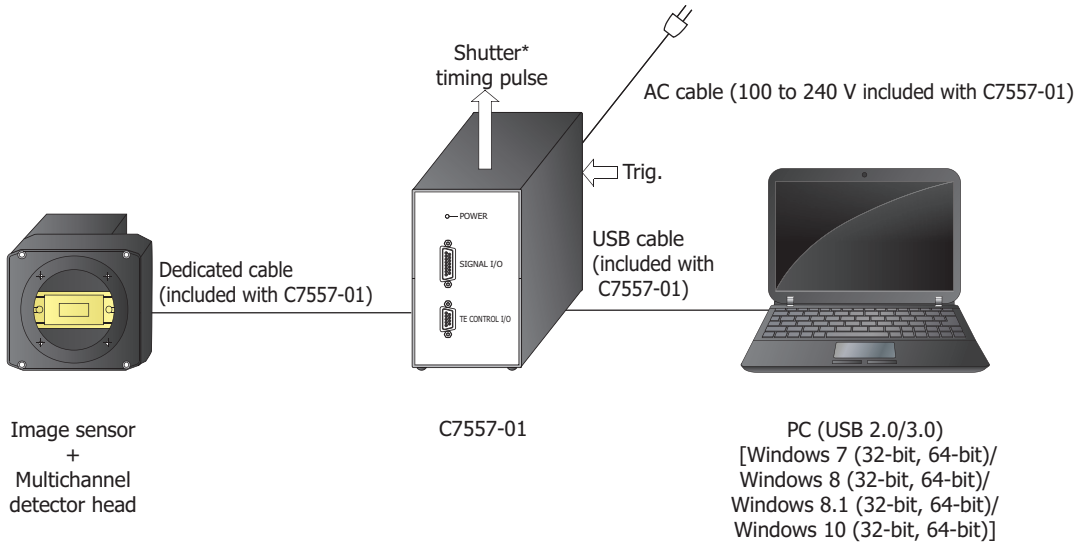
Input	Symbol	Value
Supply voltage	V_{D1}	+5 Vdc, 200 mA
	V_{A1+}	+15 Vdc, +100 mA
	V_{A1-}	-15 Vdc, -100 mA
	V_{A2}	+24 Vdc, 30 mA
	V_{D2}	+5 Vdc, 30 mA (C 7021-02, C7025-02)
	V_p	+5 Vdc, 2.5 A (C 7021-02, C7025-02)
	V_F	+12 Vdc, 100 mA (C 7021-02, C7025-02)
Master start	ϕms	HCMOS logic compatible
Master clock	ϕmc	HCMOS logic compatible, 1 MHz

Multichannel detector head controller C7557-01

Features

- **For control of multichannel detector head and data acquisition**
- **Easy control and data acquisition using supplied software via USB interface**

Connection example



* Shutter, etc. are not available.

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Cat. No. KMPD1092E06 Apr. 2019