

FlashFlex51 MCU

SST89C54 / SST89C58 / SST89C59



Advance Information

FEATURES:

- **Multi-Purpose 8-bit 8051 Family Compatible Microcontroller Unit (MCU) with Embedded SuperFlash Memory for Flexibility**
- **Fully Software and Development Toolset Compatible as well as Pin-For-Pin Package Compatible with Standard 8xC5x Microcontrollers**
- **256/256/512 Bytes Register/Data RAM**
- **20/36/68 KByte Embedded High Performance Flexible SuperFlash EEPROM**
 - One 16/32/64 KByte block (128-Byte sector size)
 - One 4 KByte block (64-Byte sector size)
 - Individual Block Security Lock
 - 87C5x Programmer Compatible
 - Concurrent Operation during In-Application Programming (IAP)
 - Memory Re-Mapping
- **Support External Address Range up to 64 KByte of Program and Data Memory**
- **High Current Drive on Port 1 (5, 6, 7) pins**
- **Three 16-bit Timer/Counter**
- **Programmable Serial Port (UART)**
- **Six Interrupt Sources at 2 Priority Levels**
- **Selectable Watchdog Timer (WDT)**
- **Four 8-bit I/O Ports (32 I/O Pins)**
- **TTL- and CMOS-Compatible Logic Levels**
- **Extended Power-Saving Modes**
 - Idle Mode
 - Power Down Mode with External Interrupt Wake-up
 - Standby (Stop Clock) Mode
- **0 to 33 MHz Operation at 5 Volts Supply**
- **Low Voltage (3V) Operation (0 to 12 MHz)**
- **PDIP-40, PLCC-44 and TQFP-44 Packages**
- **Temperature Ranges:**
 - Commercial (0°C to +70°C)
 - Industrial (-40°C to +85°C)

PRODUCT DESCRIPTION

SST89C54, SST89C58 and SST89C59 are members of the FlashFlex51 family of 8-bit microcontrollers. The FlashFlex51 family is a family of embedded microcontroller products designed and manufactured on the state-of-the-art SuperFlash CMOS semiconductor process technology.

As a member of the FlashFlex51 controller family, the SST89C54/58/59 uses the same powerful instruction set, has the same architecture, and is pin-for-pin compatible with standard 8xC5x microcontroller devices.

SST89C54/58/59 comes with 20/36/68 KByte of integrated on-chip flash EEPROM program memory using the patented and proprietary Silicon Storage Technology, Inc. (SST) CMOS SuperFlash EEPROM technology with the SST field enhancing tunneling injector split-gate memory cells. The SuperFlash memory is partitioned into 2 independent program memory blocks. The primary SuperFlash block occupies 16/32/64 KByte of internal program memory space and the secondary SuperFlash block occupies 4 KByte of SST89C54/58/59's internal program memory space. The 4 KByte secondary SuperFlash block can be mapped to the highest or lowest location of the 64 KByte address space, it can also be hidden from the program

counter and used as an independent E²-like data memory. The flash memory blocks can be programmed via a standard 87C5x OTP EPROM programmer or a standard flash EEPROM memory programmer fitted with a special adapter and firmware for SST89C54/58/59 devices. During the power-on reset, the SST89C54/58/59 can be configured as a master for source code storage or as a slave to an external host for In-Application Programming™ (IAP) operation. SST89C54/58/59 is designed to be programmed "in-place" and "in-operation" on the printed circuit board assembly for maximum flexibility.

The highly reliable, patented SuperFlash technology and memory cell have a number of important advantages for designing and manufacturing flash EEPROMs, when compared with other approaches. These advantages translate into significant cost and reliability benefits for our customers.

In addition to 20/36/68 KByte of SuperFlash EEPROM program memory on-chip, the SST89C54/58/59 can address up to 64 KByte of program memory external to the chip. The SST89C54/58 have 256 x 8 bits of on-chip RAM, and the SST89C59 has 512 x 8 bits of on-chip RAM. Up to 64 KByte of external data memory (RAM) can be addressed.



TABLE OF CONTENTS

PRODUCT FEATURES 1

PRODUCT DESCRIPTION 1

FUNCTIONAL BLOCKS 4

 Functional Block Diagram 4

 MCU Core 5

PIN ASSIGNMENTS 6

 Pin Descriptions 7

MEMORY ORGANIZATION 9

 Program Memory 9

 Memory Re-Mapping 11

Activation and Deactivation of Memory Re-Mapping 13

 Data Memory 15

 Special Function Registers (SFR) 15

CPU Related SFRs 15

Flash Memory Programming SFRs 16

Chip Operational SFRs 16

Timer/Counters SFRs 16

Interface SFRs 16

FLASH MEMORY PROGRAMMING 17

 External Host Programming Mode 17

 Product Identification 18

 External Host Mode Commands 18

 External Host Mode Clock Source 19

 Arming Command 20

 Programming a SST89C54/58/59 20

 Flash Operation Status Detection (Ext. Host Handshake) 20

 In-Application Programming Mode 24

 In-Application Programming Clock Source 24

 Setup Command 24

 In-Application Programming Commands 24

 Polling 25

TIMERS/COUNTERS 27

SERIAL I/O (UART) 27

INTERRUPT 28

 Interrupt Priority Levels 28



FlashFlex51 MCU

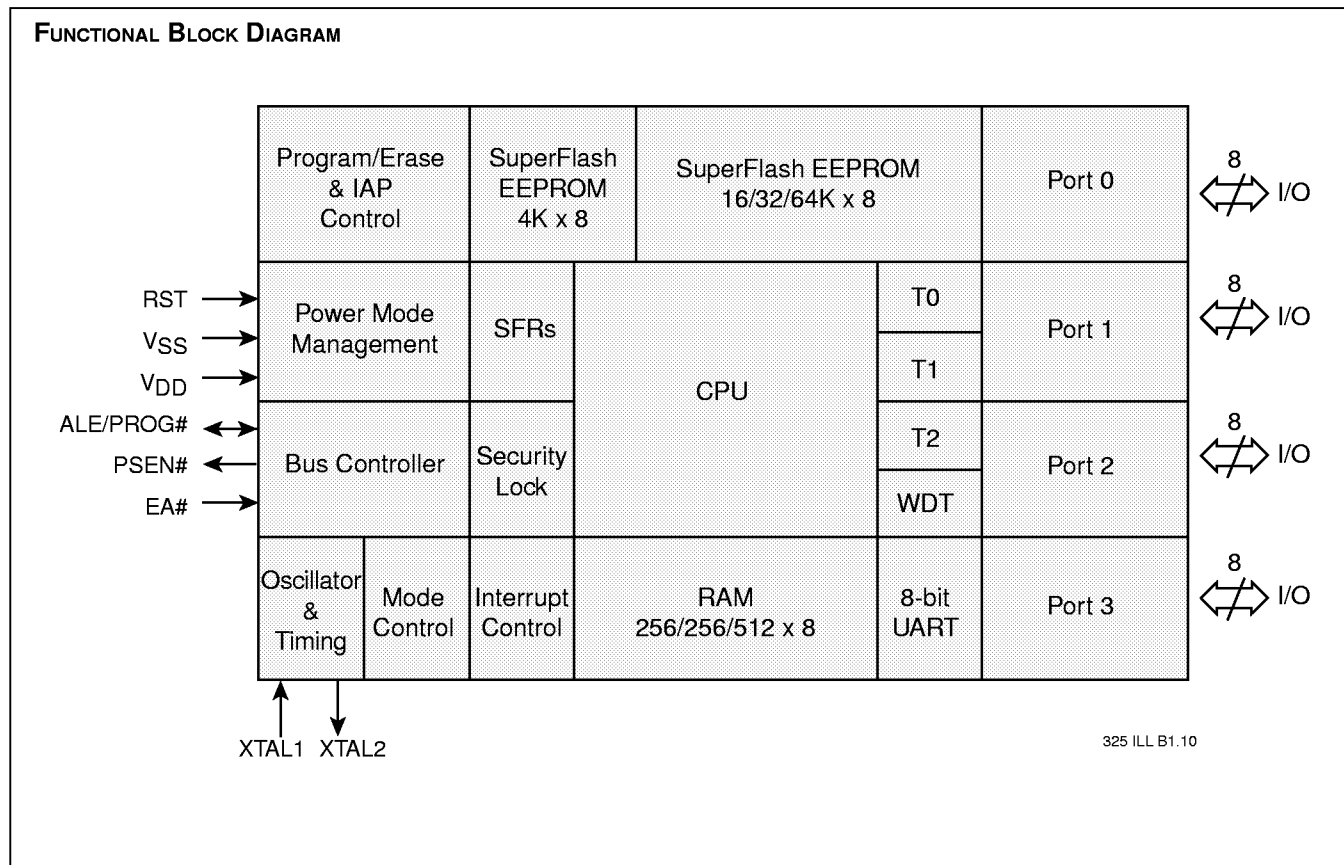
SST89C54 / SST89C58 / SST89C59

Advance Information

WATCHDOG TIMER	28
SECURITY LOCK	29
Activation and Deactivation of the Security Lock	29
<i>IAP Mode</i>	30
<i>External Host Mode</i>	30
RESET	30
Power-On Reset	30
POWER SAVING MODES	31
CLOCK INPUT OPTIONS	32
ELECTRICAL SPECIFICATION	33
Absolute Maximum Ratings	33
Operation Range	33
Reliability Characteristics	33
DC Electrical Characteristics	34
AC Electrical Characteristics	37
<i>Explanation Of Symbols</i>	38
<i>External Clock Drive</i>	39
<i>Serial Port Timing - Shift Register Mode</i>	40
PRODUCT ORDERING INFORMATION	41
Part Number Valid Combinations	42
Part Number Cross Reference Guide	43
PACKAGING DIAGRAMS	44
SALES OFFICES	48



FUNCTIONAL BLOCKS

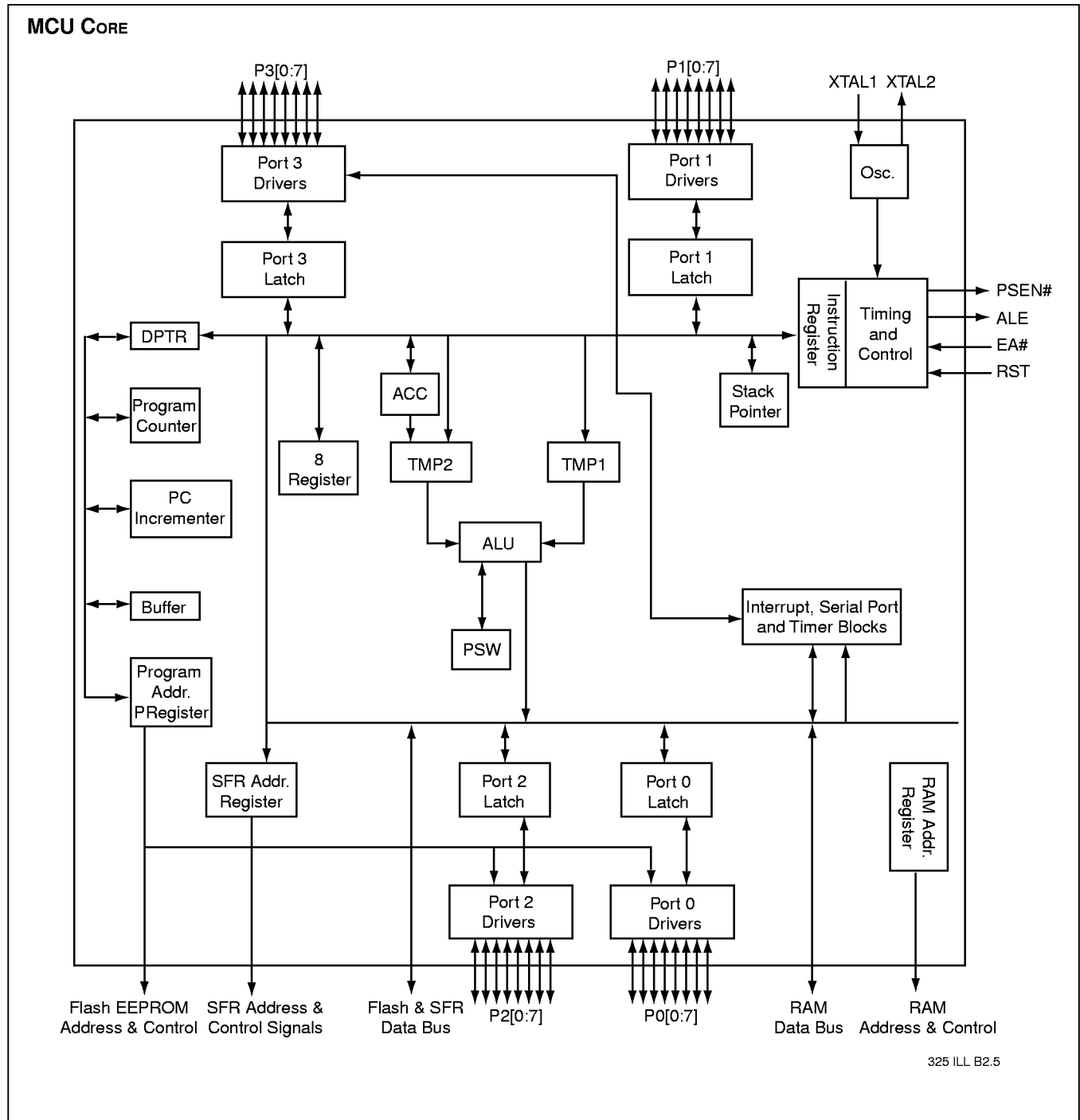




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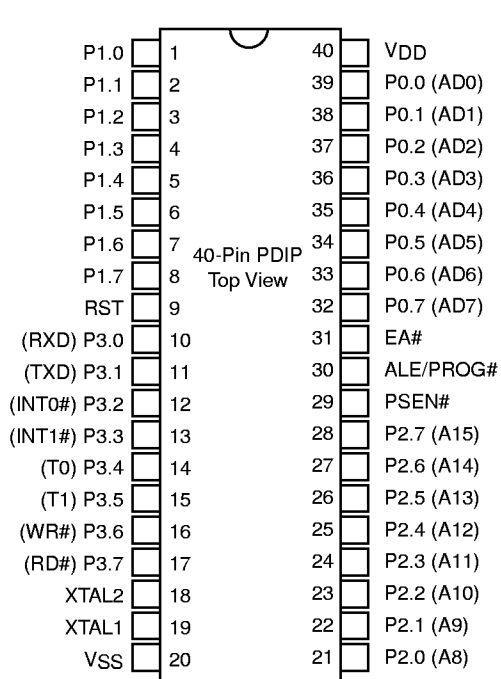
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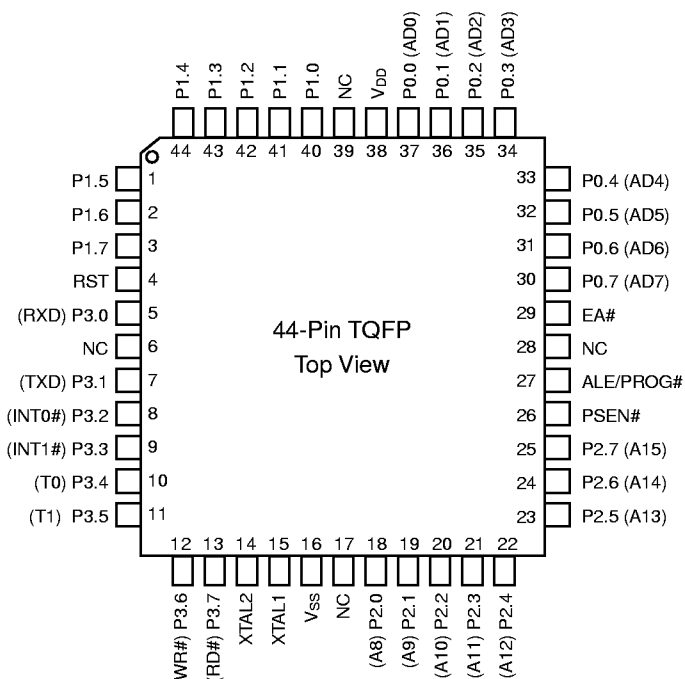




PIN ASSIGNMENTS



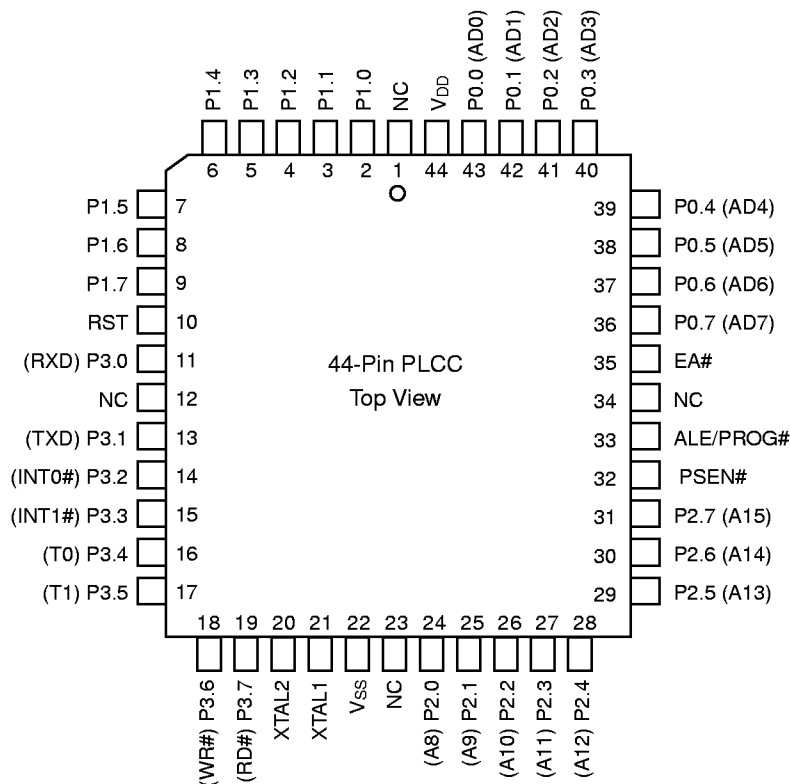
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FIGURE 1: PIN ASSIGNMENTS FOR 40-PIN PLASTIC DIP

FIGURE 2: PIN ASSIGNMENTS FOR 44-PIN TQFP



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FIGURE 3: PIN ASSIGNMENTS FOR 44-PIN PLCC

Note: NC pins must be left unconnected.



FlashFlex51 MCU

SST89C54 / SST89C58 / SST89C59

Advance Information

TABLE 1: PIN DESCRIPTIONS

Symbol	Type ¹	Name and Functions
P0[7:0]	I/O ¹	Port 0: Port 0 is an 8-bit open drain bi-directional I/O port. As an output port each pin can sink several LS TTL inputs. Port 0 pins that have 1's written to them float, and in that state can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external memory. In this application it uses strong internal pull-ups when transitioning to 1's. Port 0 also receives the code bytes during FLASH MEMORY programming, and outputs the code bytes during program verification. External pull-ups are required during program verification.
P1[7:0]	I/O with internal pull-ups	Port 1: Port 1 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 1 output buffers can drive LS TTL inputs. Port 1 pins that have 1's written to them are pulled high by the internal pull-ups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally pulled low will source current (I_{IL} , on the data sheet) because of the internal pull-ups. P1(5, 6, 7) have high current drive of 16 mA. Port 1 also receives the low-order address bytes during FLASH MEMORY programming and program verification.
P2[7:0]	I/O with internal pull-ups	Port 2: Port 2 is an 8-bit bi-directional I/O port with internal pull-ups. Port 2 pins that have 1's written to them are pulled high by the internal pull-ups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally pulled low will source current (I_{IL} , on the data sheet) because of the internal pull-ups. Port 2 sends the high-order address byte during fetches from external Program memory and during accesses to external Data Memory that use 16-bit address (MOVX@DPTR). In this application it uses strong internal pull-ups when outputting 1's. During accesses to external Data Memory that use 8-bit addresses (MOVX@Ri), Port 2 sends the contents of the P2 Special Function Register. Port 2 also receives some control signals and a partial of high-order address bits during FLASH MEMORY programming and program verification.
P3[7:0]	I/O with internal pull-ups	Port 3: Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 3 output buffers could drive LS TTL inputs. Port 3 pins that have 1's written to them are pulled high by the internal pull-ups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally pulled low will source current (I_{IL} , on the data sheet) because of the pull-ups. Port 3 also serves the functions of various special features of the FlashFlex51 Family. Port 3 also receives some control signals and a partial of high-order address bits during FLASH MEMORY programming and program verification.
P3.0	I	RXD: Serial input line
P3.1	O	TXD: Serial output line
P3.2	I	INT0#: External Interrupt 0
P3.3	I	INT1#: External Interrupt 1
P3.4	I	T0: Timer 0 external input
P3.5	I	T1: Timer 1 external input
P3.6	O	WR#: External Data Memory Write strobe
P3.7	O	RD#: External Data Memory Read strobe
PSEN#	O/I	Program Store Enable: PSEN# is the Read strobe to External Program Memory. When the SST89C54/58/59 are executing from Internal Program Memory, PSEN# is inactive (high). When the device is executing code from External Program Memory, PSEN# is activated twice each machine cycle, except that two PSEN# activations are skipped during each access to External Data Memory. While the RST input is continually held high (for more than ten machine cycles), a forced high-to-low input transition on the PSEN# pin will bring the device into the "External Host" mode for the internal flash memory programming operation.



PIN DESCRIPTIONS (CONTINUED)

Symbol	Type ¹	Name and Functions
RST	I	Reset: A high on this pin for two machine cycles while the oscillator is running resets the device. The port pins will be driven to their reset condition when a minimum V_{IH1} voltage is applied whether the oscillator is running or not. An internal pulldown resistor permits a power-on reset with only a capacitor connected to V_{DD} . After a successful reset is completed, if the PSEN# pin is driven by an input force with a high-to-low transition while the RST input pin is continually held high, the device will enter the "External Host" mode for the internal flash memory programming operation, otherwise the device will enter the "Normal" operation mode.
EA#	I	External Access Enable: EA# must be strapped to V_{SS} in order to enable the SST89C54/58/59 to fetch code from External Program Memory locations starting at 0000h up to FFFFh. Note, however, that if the Security Lock is activated on either block, the logic level at EA# is internally latched during reset. EA# must be strapped to V_{DD} for internal program execution. The EA# pin can tolerate a high voltage ² of 12V (see Electrical Specification).
ALE/PROG#	I/O	Address Latch Enable: ALE is the output signal for latching the low byte of the address during accesses to external memory. This pin is also the programming pulse input (PROG#).
XTAL ₁ XTAL ₂	I O	Oscillator: Input and output to the inverting oscillator amplifier. XTAL1 is input to internal clock generation circuits from an external clock source.
V_{DD}	I	Power Supply: Supply voltage during normal, Idle, Power Down, and Standby Mode operations.
V_{SS}	I	Ground: Circuit ground. (0V reference)

Note: 1) I = Input
O = Output

2) It is not necessary to receive a 12V programming supply voltage during flash programming.

325 PGM T1.10



FlashFlex51 MCU SST89C54 / SST89C58 / SST89C59

Advance Information

MEMORY ORGANIZATION

The SST89C54/58/59 has separate address spaces for program and data memory.

Program Memory

There are two internal flash memory blocks in the SST89C54/58/59. The primary flash memory block (Block 0) has 16/32/64 KByte and occupies the address space 0000h to 3FFFh/7FFFh/FFFFh. The secondary flash memory block (Block 1) has 4 KByte and occupies the address space F000h to FFFFh accessible through In-Application Programming.

The 16 K by 8 primary SuperFlash block is organized as 256 rows (128 of 128-Byte sections/pages, 8 X-address lines) and 512 columns (64 Bytes per row, 6 Y-address lines).

The 32 K by 8 primary SuperFlash block is organized as 512 rows (256 of 128-Byte sectors/pages, 9 X-address lines) and 512 columns (64 Bytes per row, 6 Y-address lines).

The 64 K by 8 primary SuperFlash block is organized as 1024 rows (512 of 128-Byte sectors/pages, 10 X-address lines) and 512 columns (64 Bytes per row, 6 Y-address lines).

The 4 K by 8 secondary SuperFlash block is organized as 128 rows (64 of 64-Byte sectors/pages, 7 X-address lines) and 128 columns (32 Bytes per row, 5 Y-address lines).

When internal code operation is enabled (EA# = 1), the secondary 4 KByte flash memory block is only visible during In-Application Programming operation, otherwise it is hidden from the program counter. The secondary block is accessible through the SuperFlash mailbox registers: SFCM, SFCF, SFAL, SFAH and SFDT. When bit 7 of the SuperFlash Configuration/Status mailbox register (SFCF:7), SFR address location B6h, is set, the secondary 4 KByte block will be available for code fetching.

The primary 16/32/64 KByte flash memory block is always visible to the program counter for code fetching. After the hardware resets, if the external enable is not asserted, EA# = 1, the MCU starts program execution from the lowest address space of the primary block, unless the secondary block is re-mapped to the lowest address space. Figure 4, 5 and 6 show program memory organizations for the SST89C54/58/59.

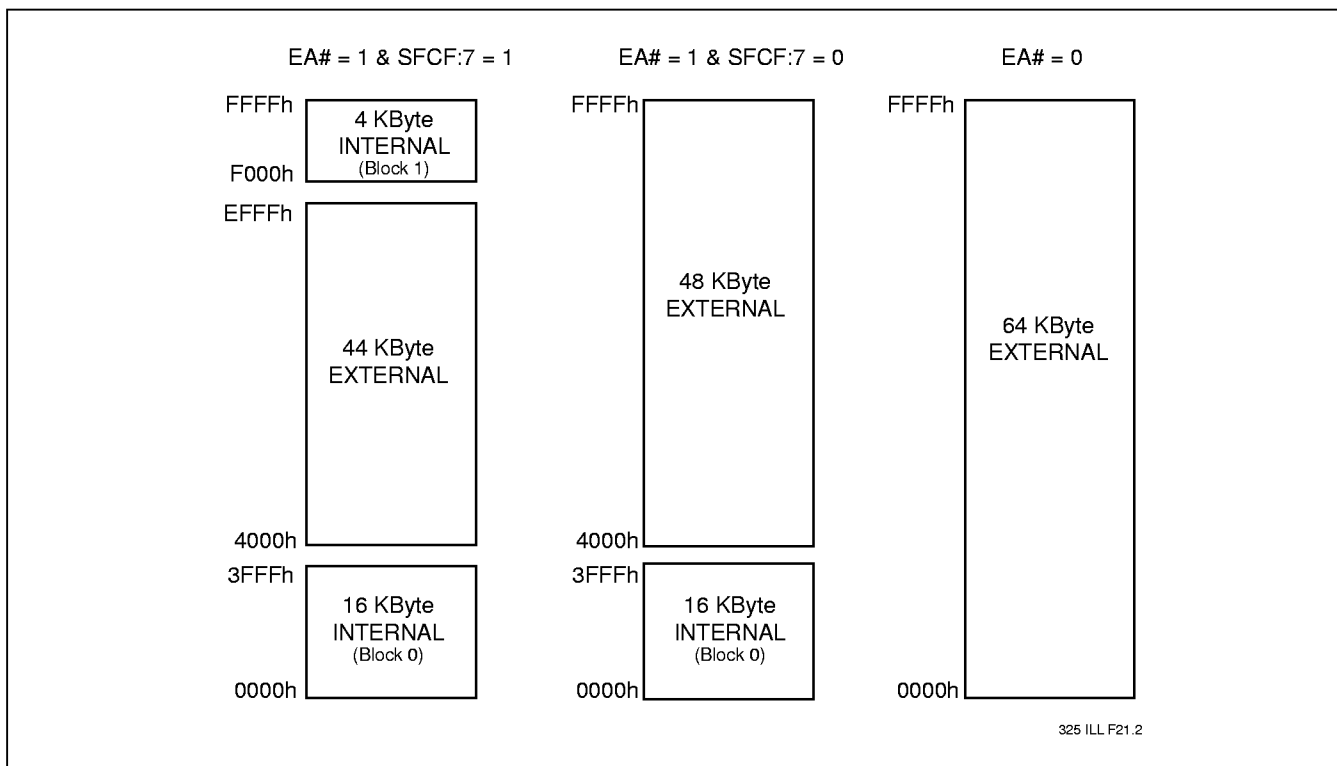


FIGURE 4: SST89C54 PROGRAM MEMORY ORGANIZATION

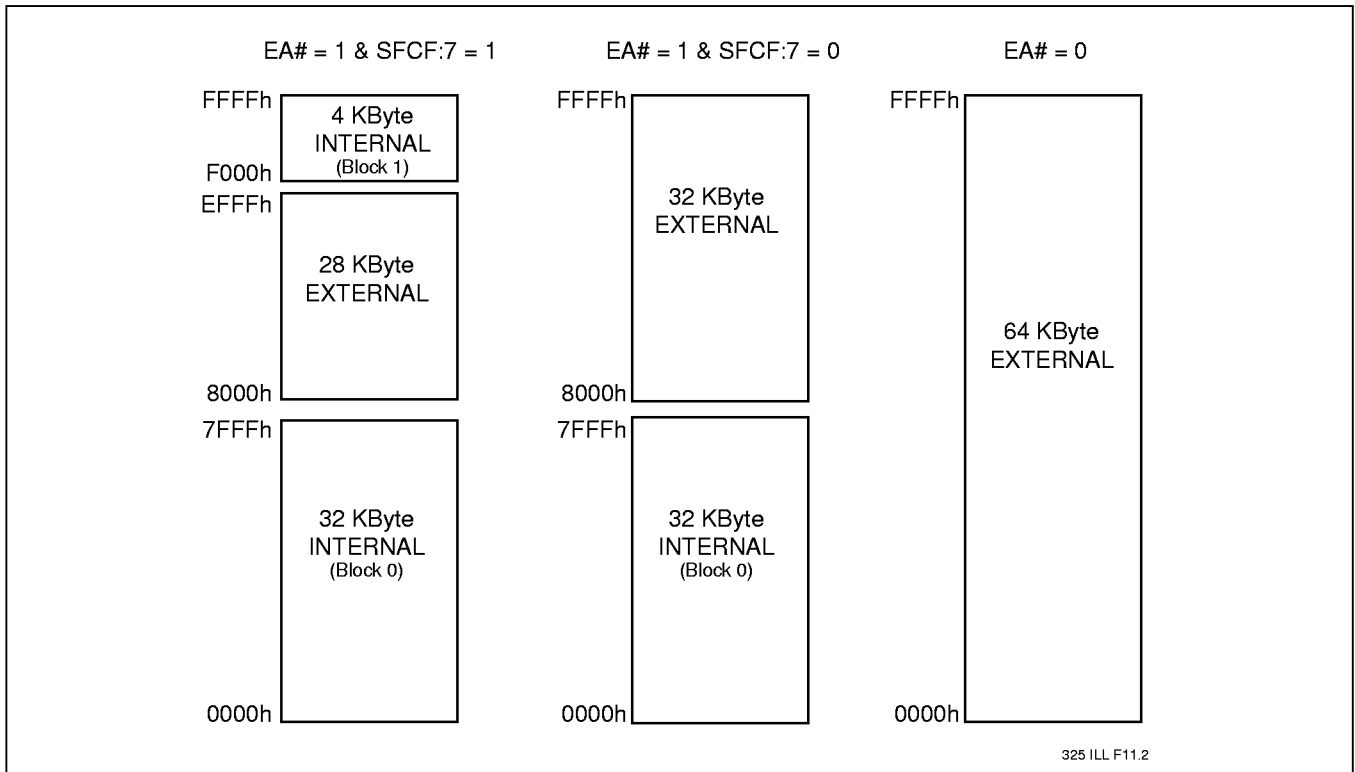


FIGURE 5: SST89C58 PROGRAM MEMORY ORGANIZATION

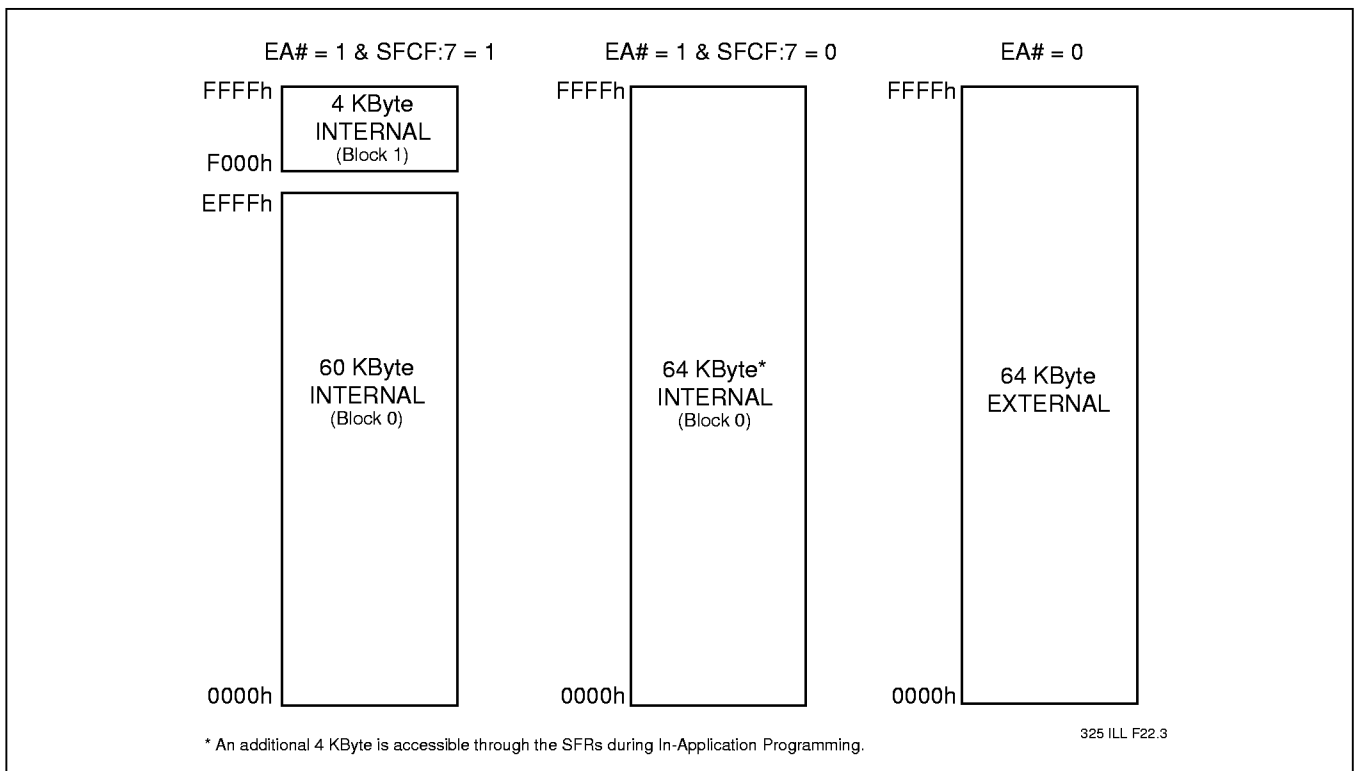


FIGURE 6: SST89C59 PROGRAM MEMORY ORGANIZATION



FlashFlex51 MCU

SST89C54 / SST89C58 / SST89C59

Advance Information

Memory Re-mapping

The SST89C54/58/59 memory re-mapping feature will allow users to reorganize the internal Flash memory sectors so that interrupts may be supported/serviced when an In-Application Programming operation is in progress. When re-mapping is enabled, up to 4 KBytes of flash memory from the Block 0 will be reassigned to overlay the address space of Block 1. If 4 KBytes are

reassigned, any flash accesses within the address range of 0000h – 0FFFh will have the uppermost 4 address bits interpreted as ones, redirecting the access to F000h–FFFFh range on the address map. Therefore, the reassigned physical flash memory will have dual (virtual) addresses. Figure 7, 8 and 9 shows re-mapped program memory organizations for SST89C54/58/59.

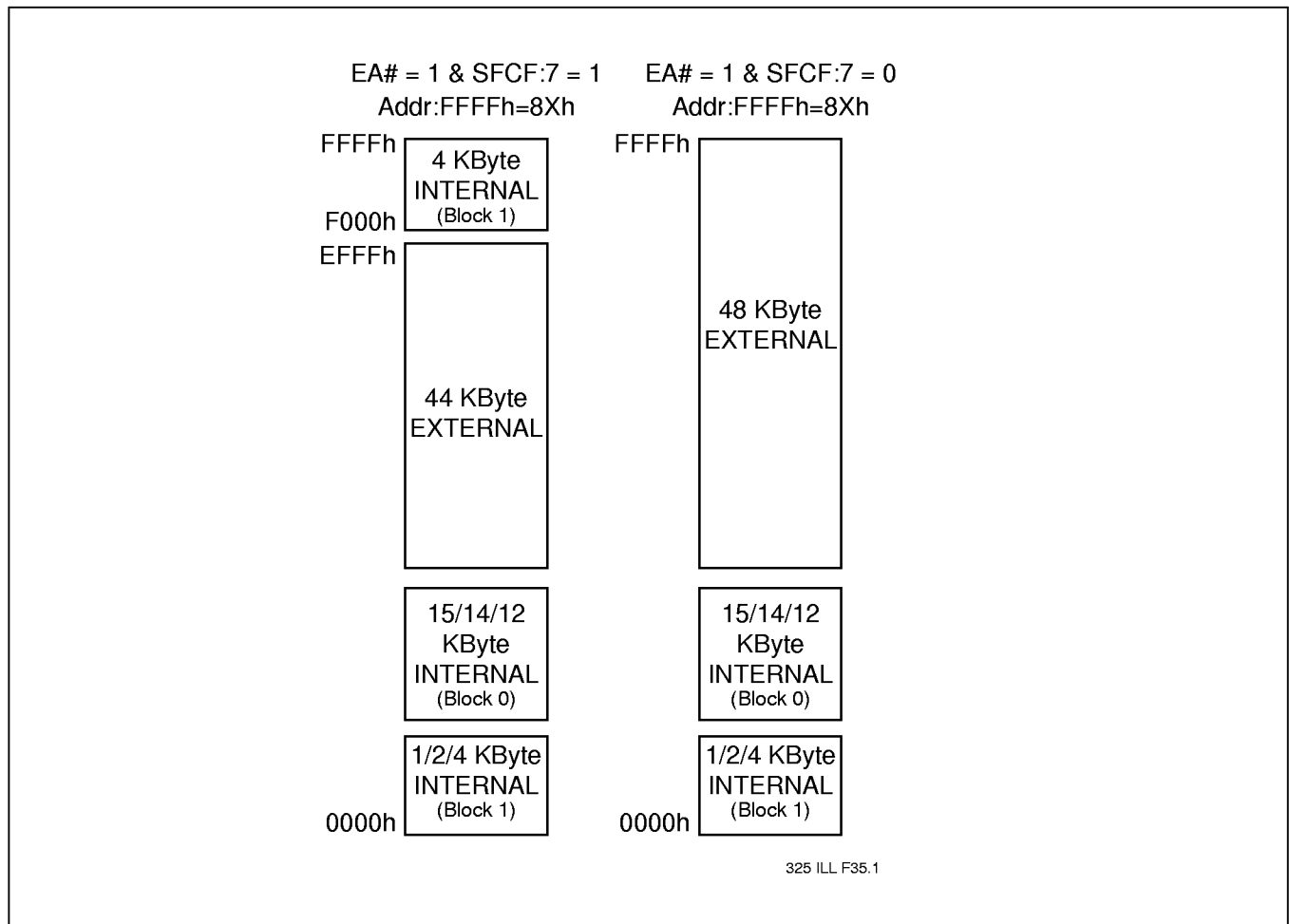


FIGURE 7: SST89C54 RE-MAPPED PROGRAM MEMORY ORGANIZATION

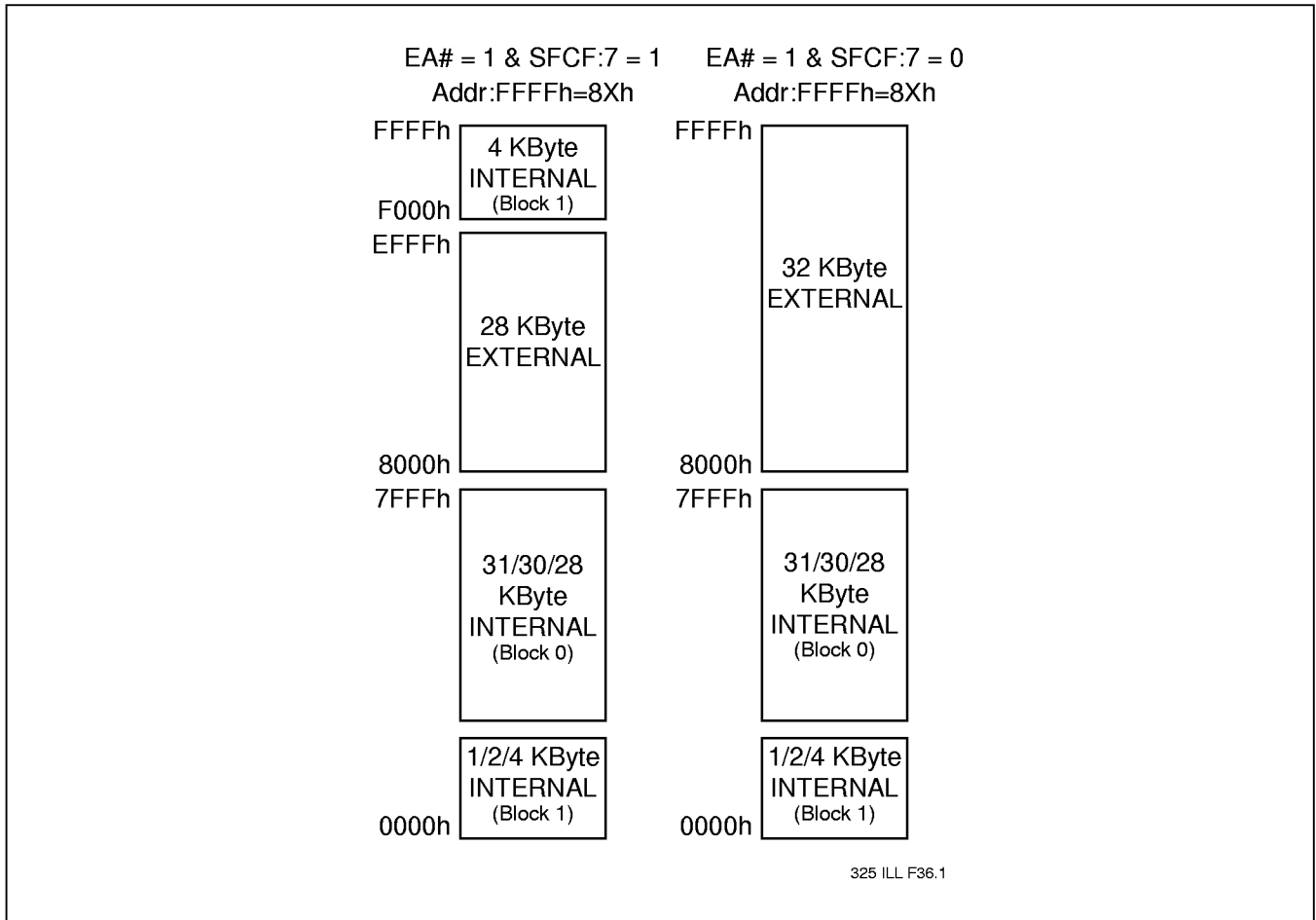


FIGURE 8: SST89C58 RE-MAPPED PROGRAM MEMORY ORGANIZATION



FlashFlex51 MCU

SST89C54 / SST89C58 / SST89C59

Advance Information

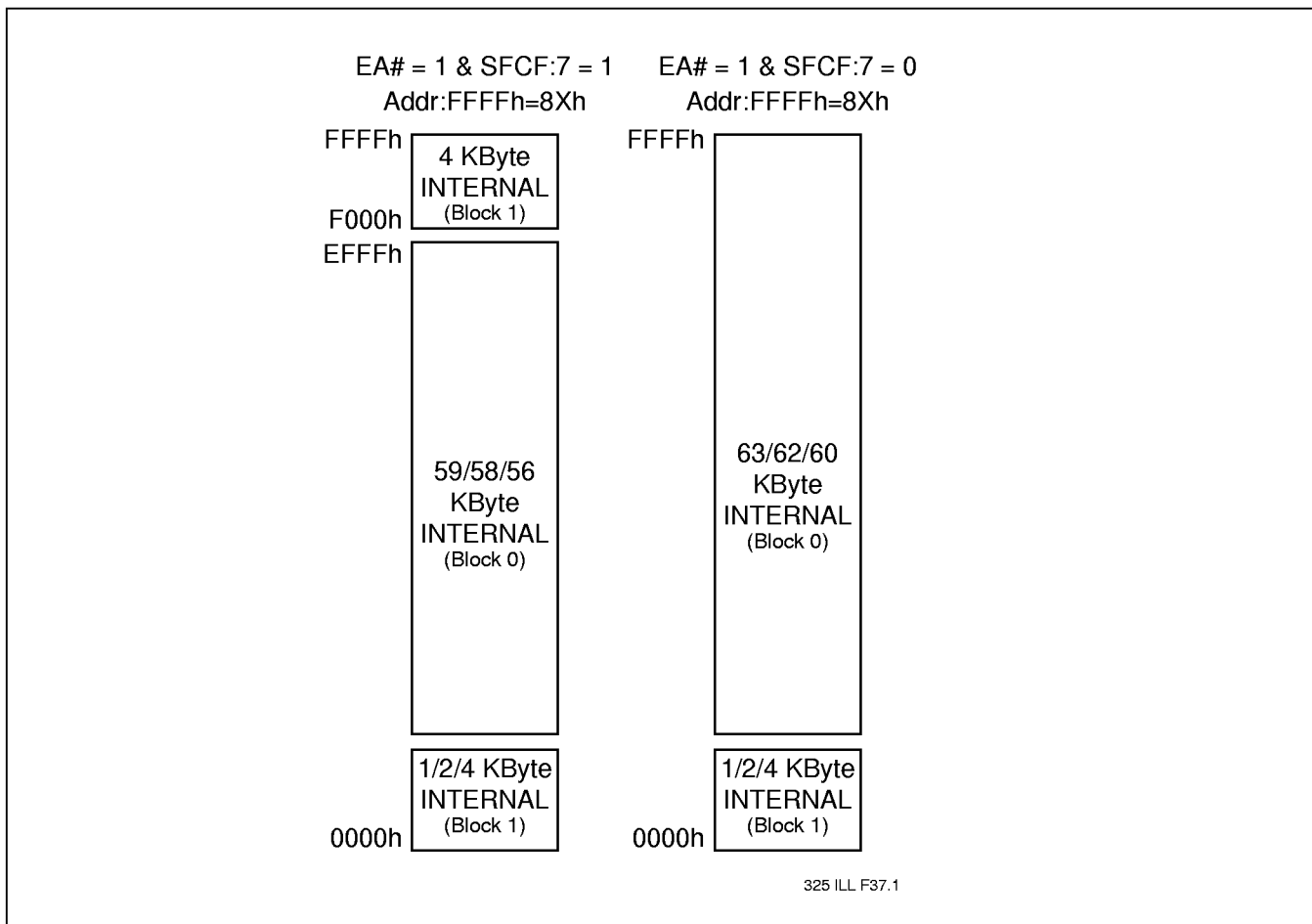


FIGURE 9: SST89C59 RE-MAPPED PROGRAM MEMORY ORGANIZATION

Activation and Deactivation of Memory Re-mapping

The Re-Map Enable Control (RMEC) bit located in bit [7] of Flash memory location FFFFh activates the Re-mapping feature. A “0” programmed to the RMEC location turns on re-mapping. A “1” disables all re-mapping and both flash memory blocks addresses return to its original configuration. The Re-map [1:0] bits, in flash memory location FFDFh determines the size of the memory sector to be remapped. Figure 10 shows the location of REMC and Re-Map bits. Re-mapping will be initialized according to the contents in REMC and Re-Map [1:0] bits after a successful reset. See Table 2. Once the device completes the reset initialization process, altering the contents of REMC and Re-Map bits will

only take effect at the next MCU reset. The configuration of the re-mapped memory may be altered at any time after a Power-On Reset by programming the MAP_EN byte located in the SFCF [1:0] register with value listed in Table 2.

To deactivate memory re-mapping, a CHIP ERASE operation will reprogram the REMC bit with a “1”, and disabling the re-mapping feature. Programming 00h to the SFCF [1:0] register through In-Application Programming Mode may also deactivate memory Re-mapping, note that upon the next reset, the contents on REMC and Re-Map [1:0] will again determine the contents of SFCF [1:0].

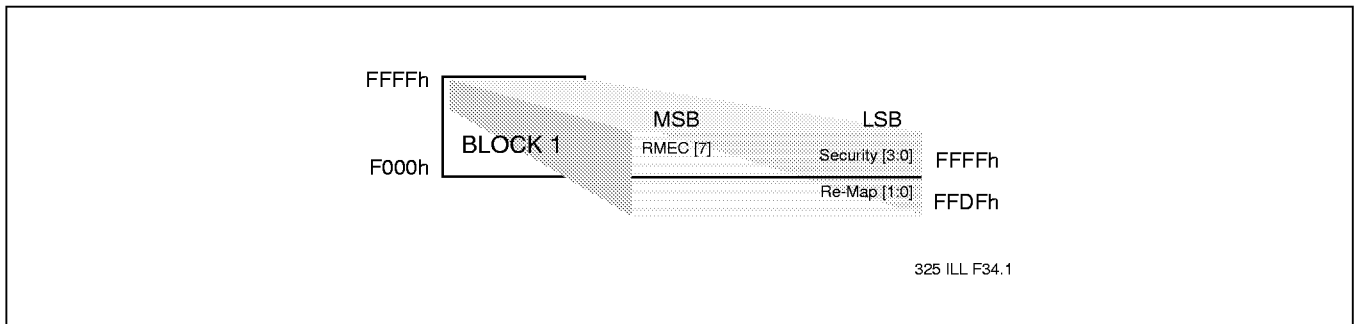


FIGURE 10: LOCATION OF REMC AND RE-MAP BITS

TABLE 2: RE-MAPPING TABLE

REMC ^{1,4}	Re-Map [1:0] ^{2,4}	MAP_EN ^{3,5}	Comments
1	XX	00	Re-mapping is turned off. Program memory is in normal configuration
0	11		
0	10	01	1 KByte of flash memory location is re-mapped. Address location 0000h-03FFh is re-mapped to F000h – F3FFh.
0	01	10	2 KBytes of flash memory location are re-mapped. Address location 0000h-07FFh is re-mapped to F000h – F7FFh.
0	00	11	4 KBytes of flash memory location is re-mapped. Address location 0000h-0FFFh is re-mapped to F000h – FFFFh.

¹ Re-Map Enable Control (REMC) is bit [7] of flash memory address location FFFFh.

² Re-Map [1:0] are the lowest bits in flash memory address FFDFh.

³ MAP_EN bits are located in the SFR SuperFlash Configuration/Status register, SFCF [1:0].

⁴ Re-mapping will be enabled according to the contents of REMC and Re-Map during the reset process.

⁵ Re-mapping configuration may be altered through the SFCF [1:0] register during In-Application Programming after power up.



FlashFlex51 MCU

SST89C54 / SST89C58 / SST89C59

Advance Information

Data Memory

SST89C54/58/59 have 256/256/512 x 8 bits on chip RAM and can address up to 64 KByte of off-chip data memory.

Special Function Registers (SFR)

Most of the unique features of the FlashFlex51 microcontroller family are controlled by bits in special function registers (SFRs) located in the FlashFlex51 SFR Memory Map shown below. Individual descriptions of each SFR are provided and Reset values indicated in Tables 3A to 3E.

8 BYTES

F8											FF
F0	B*										F7
E8											EF
E0	ACC*										E7
D8											DF
D0	PSW*										D7
C8	T2CON*		RCAP2L	RCAP2H	TL2	TH2					CF
C0	WDTC										C7
B8	IP*										BF
B0	P3*		SFCM	SFAL	SFAH	SFDT	SFCF				B7
A8	IE*										AF
A0	P2*										A7
98	SCON*	SBUF									9F
90	P1*										97
88	TCON*	TMOD	TL0	TL1	TH0	TH1					8F
80	P0*	SP	DPL	DPH				WDTD	PCON		87

FlashFlex51 SFR Memory Map

* = BIT ADDRESSABLE

All addresses are hexadecimal

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SST89C54/58/59 Special Function Registers

TABLE 3A: CPU RELATED SFRs

Symbol	Description	Direct Address	Bit Address, Symbol, or Alternative Port Function								RESET Value
			MSB				LSB				
ACC*	Accumulator	E0h	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0	00h
B*	B Register	F0h	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0	00h
PSW*	Program Status Word	D0h	CY	AC	F0	RS1	RS0	OV	F1	P	00h
SP	Stack Pointer	81h	SP[7:0]								07h
DPL	Data Pointer Low 0	82h	DPL[7:0]								00h
DPH	Data Pointer High 0	83h	DPH[7:0]								00h
IE*	Interrupt Enable	A8h	EA	-	ET2	ES0	ET1	EX1	ET0	EX0	00h
IP*	Interrupt Priority	B8h	-	-	PT2	PS	PT1	PX1	PT0	PX0	xx00000B

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TABLE 3B: FLASH MEMORY PROGRAMMING SFRs

Symbol	Description	Direct Address	Bit Address, Symbol, or Alternative Port Function						RESET Value
			MSB			LSB			
SFCF	SuperFlash Configuration/Status	B6h	VIS	SECD	-	BUSY	-	MAP_EN	00h
SFCM	SuperFlash Command	B2h	FIE	FCM					00h
SFDT	SuperFlash Data	B5h	SuperFlash Data Register						00h
SFAL	SuperFlash Address Low	B3h	SuperFlash Low Order Byte Address Register – A7 to A0 (SFAL)						00h
SFAH	SuperFlash Address High	B4h	SuperFlash High Order Byte Address Register – A15 to A8 (SFAH)						00h

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TABLE 3C: CHIP OPERATIONAL SFRs

PCON	Power Control	87h	SMOD	-	-	-	GF1	GF0	PD	IDL	0xxx0000B
WDTC	Watchdog Timer Control	C0h	-	-	-	-	WDRE	WDTS	WDT	SWDT	X0h
WDTD	Watchdog Timer Data/Reload	86h	WDRL							00h	

325 PGM T9C.2

TABLE 3D: TIMER/COUNTERS SFRs

Symbol	Description	Address	Timer 1				Timer 0				RESET Value
			GATE	C/T#	M1	M0	GATE	C/T#	M1	M0	
TMOD	Timer/Counter Mode Control	89h									00h
TCON*	Timer / Counter Control	88h	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00h
TH0	Timer 0 MSB	8Ch	TH0[7:0]								00h
TL0	Timer 0 LSB	8Ah	TL0[7:0]								00h
TH1	Timer 1 MSB	8Dh	TH1[7:0]								00h
TL1	Timer 1 LSB	8Bh	TL1[7:0]								00h
T2CON*	Timer / Counter 2 Control	C8h	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2#	CP/RL2#	00h
TH2	Timer 2 MSB	CDh	TH2[7:0]								00h
TL2	Timer 2 LSB	CCh	TL2[7:0]								00h
RCAP2H	Timer 2 Capture MSB	CBh	RCAP2H[7:0]								00h
RCAP2L	Timer 2 Capture LSB	CAh	RCAP2L[7:0]								00h

325 PGM T9D.0

TABLE 3E: INTERFACE SFRs

Symbol	Description	Address	SBUF[7:0]								RESET Value
SBUF	Serial Data Buffer	99h									Indeterminate
SCON*	Serial Port Control	98h	SM0	SM1	SM2	REN	TB8	RB8	T1	R1	00h
P0*	Port 0	80h	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0	FFh
P1*	Port 1	90h	-	-	-	-	-	-	T2EX	T2	FFh
P2*	Port 2	A0h	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0	FFh
P3*	Port 3	B0h	RD#	WR#	T1	T0	INT1#	INT0#	TXD0	RXD0	FFh

* SFRs are bit addressable

325 PGM T9E.0



FlashFlex51 MCU

SST89C54 / SST89C58 / SST89C59

Advance Information

FLASH MEMORY PROGRAMMING

The SST89C54/58/59 internal flash memory can be programmed or erased using the following two methods:

- External Host Mode (parallel only)
- In-Application Programming (IAP) Mode (parallel or serial)

EXTERNAL HOST PROGRAMMING MODE

The SST89C54/58/59 provide the user with a direct flash memory access that can be used for programming into the flash memory without using the CPU. The direct flash memory access is entered using the External Host Mode. While the reset input (RST) is continually held active (high), if the PSEN# pin is forced by an input with a transition from high-to-low state, the device enters the External Host Mode arming state at this time. The CPU core is stopped from running and all the chip I/O pins are reassigned and become flash memory access and control pins. At this time, the external host should initiate a "READ-ID" operation. After the completion of the "READ-ID" operation, the device is armed and enters the External Host Mode. After the device enters into the External Host Mode, the internal flash memory blocks are accessed through the re-assigned I/O port pins (please see Figure 11 for details) by an external host, such as a printed circuit board tester, a PC controlled development board or an OTP MCU programmer.

When the chip is in the external host mode, Port 0 pins are assigned to be the parallel data input and output pins.

Port 1 pins are assigned to be the non-muxed low order address bus signals for the internal flash memory (A0-A7). The first six bits of Port 2 pins (P2[0:5]) are assigned to be the non-muxed upper order address bus signals for the internal flash memory (A8-A13) along with two of the Port 3 pins (P3.4 as A14 and P3.5 as A15). Two upper order Port 2 pins (P2.6 and P2.7) and two upper order Port 3 pins (P3.6 and P3.7) along with RST, PSEN#, PROG#/ALE, EA# pins are assigned as the control signal pins. The Port 3 pin (P3.3) is assigned to be the ready/busy status signal, which can be used for handshaking with the external host during a flash memory programming operation. The flash memory programming operation (Erase, Program, Verify, etc.) is internally self-timed and can be controlled by an external host asynchronously or synchronously.

The insertion of an "arming" command prior to entering the External Host Mode by utilizing the "READ ID" operation provides additional protection for inadvertent writes to the internal flash memory cause by a noisy or unstable system environment during the power-up or brown-out condition.

The External Host Mode uses seven (7) hardware commands, which are decoded from the control signal pins, to facilitate the internal flash memory erase, test and programming process. The External Host Mode is enabled on the falling edge of PSEN#. The External Host Mode Commands are enabled on the falling edge of ALE/PROG#. The list in Table 4 outlines all the commands and its control signal assignment.

TABLE 4: EXTERNAL HOST MODE COMMANDS

Operation	RST	PSEN#	PROG# /ALE	EA#	P2.6	P2.7	P3.6	P3.7	P0[7:0]	P1[7:0]	P3[5:4] P2[5:0]
READ ID	H	L	H	H	L	L	L	L	DO	AL	AH
CHIP ERASE	H	L	↓	H	H	H	H	L	X	X	X
BLOCK ERASE	H	L	↓	H	H	H	H	H	X	X	A15
SECTOR ERASE	H	L	↓	H	H	H	L	H	X	AL	AH
BYTE PROGRAM	H	L	↓	H	L	H	H	H	DI	AL	AH
BURST PROGRAM	H	L	↓	H	L	H	L	H	DI	AL	AH
VERIFY (Read) BYTE	H	L	H	H	L	L	H	H	DO	AL	AH

325 PGM T2.7

Note: Symbol ↓ signifies a negative pulse and the command is asserted during the low state of PROG#/ALE input. All other combinations of the above input pins are invalid and may result in unexpected behaviors.

Note: IntEn = Interrupt Enable for flash operation completion;
L = Logic low level; H = Logic high level; X = Don't care; AL = Address low order byte; AH = Address high order byte;
DI = Data Input; DO = Data Output; A15 = Only care for the MSB, i.e. address bit #15.

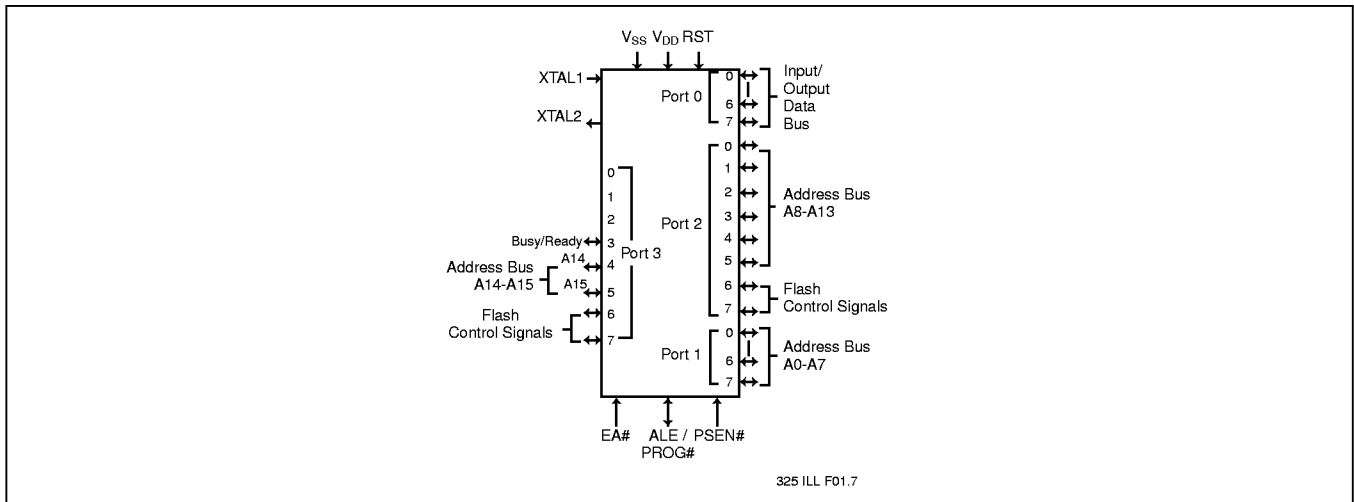


FIGURE 11: I/O PINS ASSIGNMENT FOR EXTERNAL HOST MODE

Product Identification

The READ ID command accesses the Signature Bytes that identifies the device as an SST89C54/58/59 and the manufacturer as SST. External programmers primarily use these Signature Bytes, shown in Table 5, in the selection of programming algorithms. The Read ID command is selected by the byte code of 00h on P2[6:7] and P3[6:7]. See Figure 12 for timing waveforms.

TABLE 5: SIGNATURE BYTES TABLE

	Address	Data
Manufacturer's Code	30h	BFh
SST89C54 Device Code	31h	E4h
SST89C58 Device Code	31h	E2h
SST89C59 Device Code	31h	E7h

325 GPM T3.3

External Host Mode Commands

The seven SST89C54/58/59 External Host Mode Commands are READ ID, CHIP ERASE, BLOCK ERASE SECTOR ERASE, BYTE PROGRAM, BURST PROGRAM, and VERIFY BYTE. The following is a brief description of the commands. See Table 4 for all signal logic assignments and Table 7 for all timing parameter values for the External Host Mode Commands. The critical timing for all Erase and Program commands, is self-generated by the flash memory controller on-chip. The high-to-low transition of the PROG# signal initiates the Erase and Program commands, which are synchronized internally. The Read commands are static reads, independent of the PROG# signal level.

The following three commands are for erasing all or part of the memory array. All the data in the memory array will be erased to FFh. Memory addresses that are to be

programmed must be in the erased state prior to programming. Selection of the Erase command to use, prior to programming the device, will be dependent upon the contents already in the array and the desired programming field size.

The CHIP ERASE command erases all bytes in both memory blocks (16/32/60K and 4K) of the SST89C54/58/59. This command ignores the Security Lock status and will erase the Security Byte. The CHIP ERASE command is selected by the byte code of 0Eh on P2[6:7] and P3[6:7]. See Figure 13 for timing waveforms.

The BLOCK ERASE command erases all bytes in one of the memory blocks (16/32/60K or 4K) of the SST89C54/58/59. This command will not enable if the Security Byte is enabled on the selected memory block. The selection of the memory block to be erased is determined by A15 (P3.5). If A15 is a "0", then the primary flash memory block (16/32/60K) is selected. If A15 is a "1", then the secondary flash memory block (4K) is selected. The BLOCK ERASE command is selected by the byte code of 0Fh on P2[6:7] and P3[6:7]. See Figure 14 for the timing waveforms.

The SECTOR ERASE command erases all of the bytes in a sector. The sector size for the primary flash memory (Address buffer locations 0-3FFFh/7FFFh/FFFFh) is 128 Bytes. The sector size for the secondary flash memory (Address buffer locations F000h-FFFFh) is 64 bytes. This command will not enable if the Security Byte is enabled on the selected memory block. The selection of the memory sector to be erased is determined by P2[0:5] (A8-A13) and P3[4:5] (A14 & A15). The SECTOR ERASE command is selected by the byte code of 0Dh on P2[6:7] and P3[6:7]. See Figure 15 for timing waveforms.



FlashFlex51 MCU SST89C54 / SST89C58 / SST89C59

Advance Information

The following two Program commands are for programming new data into the memory array. Selection of which Program command to use for programming will be dependent upon the desired programming field size. The Program commands will not enable if the Security Byte is enabled on the selected memory block.

The BYTE PROGRAM command programs data into a single byte. Ports P0[0:7] are used for data in. The memory location is selected by P1[0:7], P2[0:5], and P3[4:5] (A0-A15). The BYTE PROGRAM command is selected by the byte code of 07h on P2[6:7] and P3[6:7]. See Figure 16 for timing waveforms.

The BURST PROGRAM command programs data to an entire row, sequentially byte by byte. Ports P0[0:7] are used for data in. The memory location is selected by P1[0:7], P2[0:5], and P3[4:5] (A0-A15). The BYTE PROGRAM command is selected by the byte code of 05h on P2[6:7] and P3[6:7]. See Figure 17 for timing waveforms.

The VERIFY BYTE command allows the user to verify that the SST89C54/58/59 correctly performed an Erase or Program command. Ports P0[0:7] are used for data out. The memory location is selected by P1[0:7], P2[0:5], and P3[4:5] (A0-A15). This command will not enable if the Security Byte is enabled on the selected memory block. See Figure 18 for timing waveforms.

If an External Host Mode Command is issued to a secured memory block, the device will immediately reset and be ready for another command.

External Host Mode Clock Source

During External Host Mode, an internal oscillator will provide clocking for the SST89C54/58/59. The on-chip oscillator will be turned on as the SST89C54/58/59 enters External Host Mode; i.e. when PSEN goes low while RST is high. The oscillator will have a center frequency of 10 MHz and will provide both clocking for the Flash Control Unit as well as timing references for Program and Erase operations. During External Host Mode, the controller core is being held in reset. Upon exit of External Host Mode, the internal oscillator is turned off.

The same oscillator also provides time base for the watchdog timer and timing references for IAP Mode Program and Erase operations. See more detailed description in later sections.

Arming Command

An arming command must take place before External Host Commands will be recognized by the SST89C54/58/59. This is to prevent accidental triggering of External Host Commands due to noise or programmer error. The arming command is as follows:

1. PSEN# goes low while RST is high. This will get the machine in External Host Mode, re-configuring the pins.
2. A Read_ID command is issued and held for 1 ms. This is actually a natural step for the programmer, but will also serve as the arming command.

After the above sequence, all other External Host Mode commands are enabled. Before the Read_ID command is received, all other External Host commands received are ignored.

Programming a SST89C54/58/59

To program new data into the memory array, supply 5 volts to V_{DD} and RST, and perform the following steps.

1. Enable RST, and PSEN# in sequence per the appropriate timing diagram.
2. Raise EA# High (either V_{IH} or V_H).
3. Read the device and manufacturer ID using the READ ID command to ensure the correct programming algorithm.
4. Verify that the memory blocks or sectors for programming is in the erased state, FFh. If they are not erased, then erase them using the appropriate Erase command.
5. Select the memory location using the address lines (P1[0:7], P2[0:5], P3[4:5]).
6. Present the data in on P0[0:7].
7. Pulse ALE/PROG#.
8. Wait for low to high transition on READY/BUSY# (P3(3)).
9. Repeat steps 5 – 8 until programming is finished.
10. Verify the flash memory contents.

Flash Operation Status Detection (Ext. Host Handshake)

The SST89C54/58/59 provide two firmware means for an external host to detect the completion of a flash memory operation, therefore the external host can optimize the system Program or Erase cycle of the embedded flash memory. The end of a flash memory operation cycle (Erase or Program) can be detected by: 1) monitoring the Ready/Busy# bit at Port 3.3; 2) monitoring the Data# Polling bit at Port 0.7 or Port 0.3.



Ready/Busy# (P3.3)

The progress of the flash memory programming can be monitored by the Ready/Busy# output signal. P3.3 is driven low, sometime after ALE/PROG# goes low during a flash memory operation to indicate the Busy# status of the flash programming controller. P3.3 is driven high when the flash programming operation is completed to indicate the Ready status.

During a Burst Program operation, P3.3 is driven high (Ready) in between each Byte Program among the Burst Programs to indicate the ready status to receive the next byte. When the external host detects the Ready status after a byte among the burst is programmed, it may then put the data/address (in the same page) of the next byte on the bus and drive ALE/PROG# low (pulse) immediately, before the time-out limit expires

Data# Polling (P0.7 & P0.3)

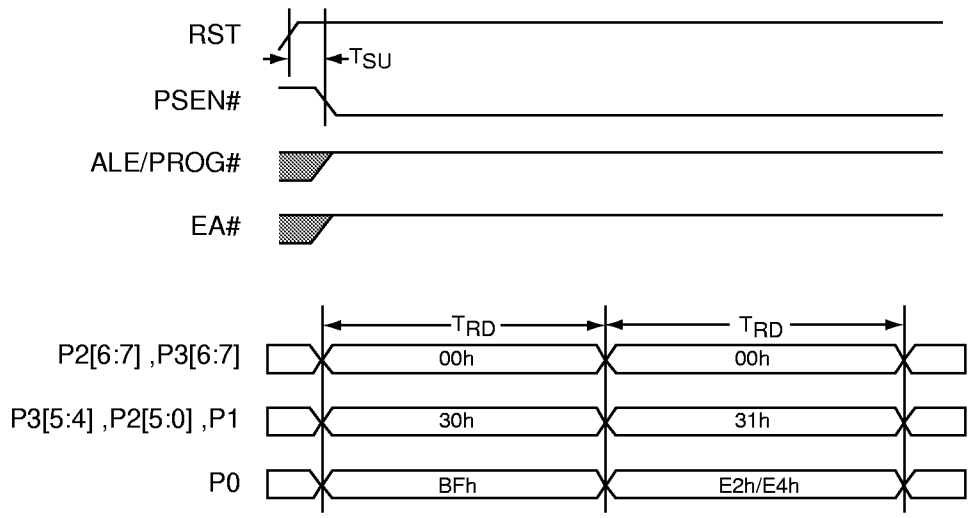
During a Burst Program operation, any attempts to read (Verify Byte), while the device is busy programming the byte among the Burst Programs, will receive the complement of the data of the last byte programmed (logic low,

i.e. "0" for an erase) on P0.3 and P0.7 with the rest of the bits "0". During a Burst Program operation, the Verify Byte command is reading the data of the last byte programmed, not the data at the address specified.

The true data will be read from P0.7, when the device completes each Byte Program among the Burst Programs to indicate the Ready status to receive the next byte. When the external host detects the Ready status after a byte among the burst is programmed, it should then put the data/address (in the same page) of the next byte on the bus and drive ALE/PROG# low (pulse) immediately, before the time-out limit expires (See programming time spec. for details.). The true data will be read from P0.3, when the Burst Program command is terminated and the device is ready for the next operation.

The termination of the Burst Program can be accomplished by: 1) Change to a new X-Addresses (Note: the X-Address range are different for the 4Kx8 flash block and for the 16/32/60K x 8 flash block.); 2) Change to a new command that requires a negative transition of the ALE/PROG# (i.e. any Erase or Program command); 3) Wait for time out limit expires (20 μs); when programming the next byte.

Flash Memory Programming with External Host Mode (Figures 12-18)



325 ILL F02.10

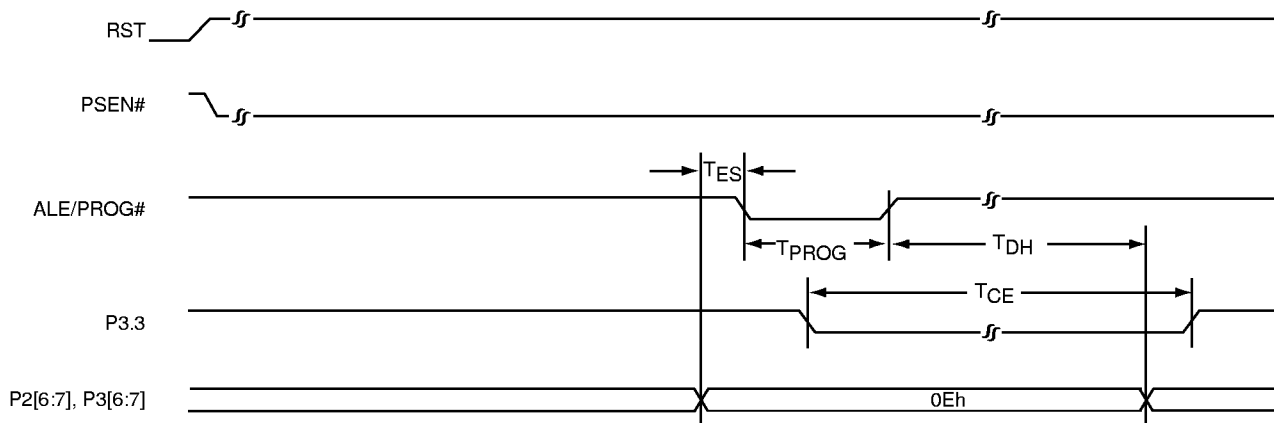
FIGURE 12: READ ID

Read chip signature and identification registers at the addressed location.



FlashFlex51 MCU SST89C54 / SST89C58 / SST89C59

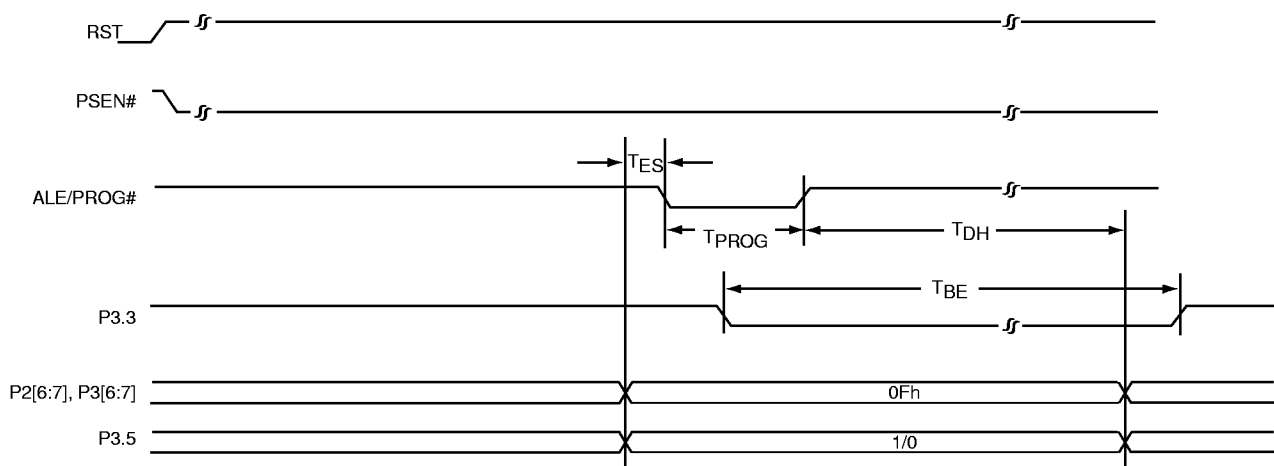
Advance Information



325 ILL F03.11

FIGURE 13: CHIP ERASE

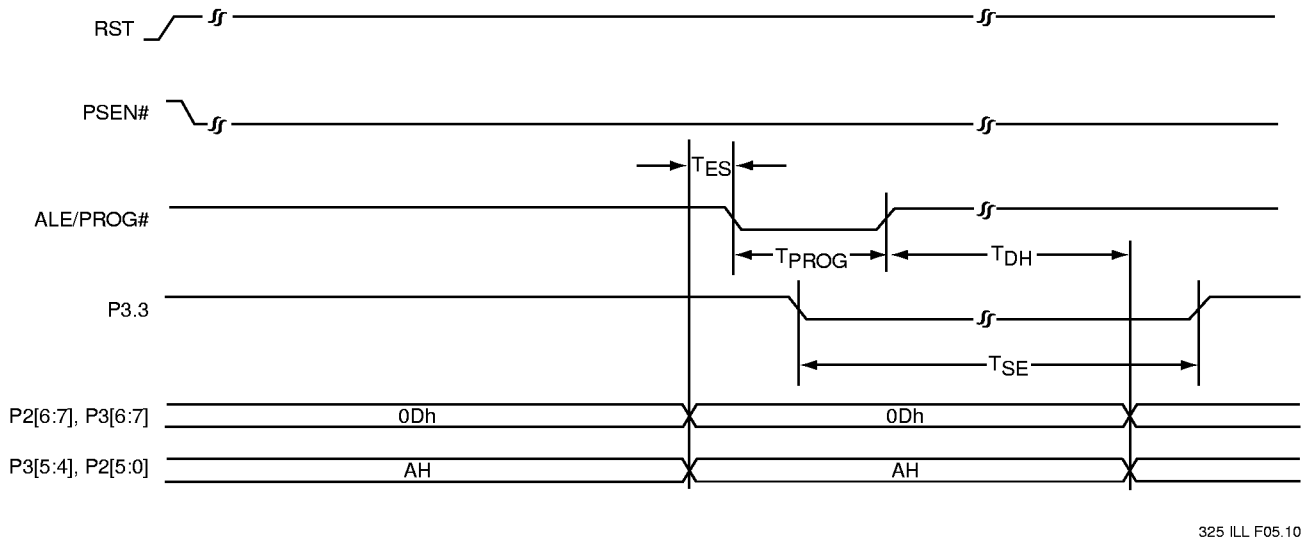
Erase both flash memory blocks. Security lock is ignored and the security byte is erased too.



325 ILL F04.11

FIGURE 14: BLOCK ERASE

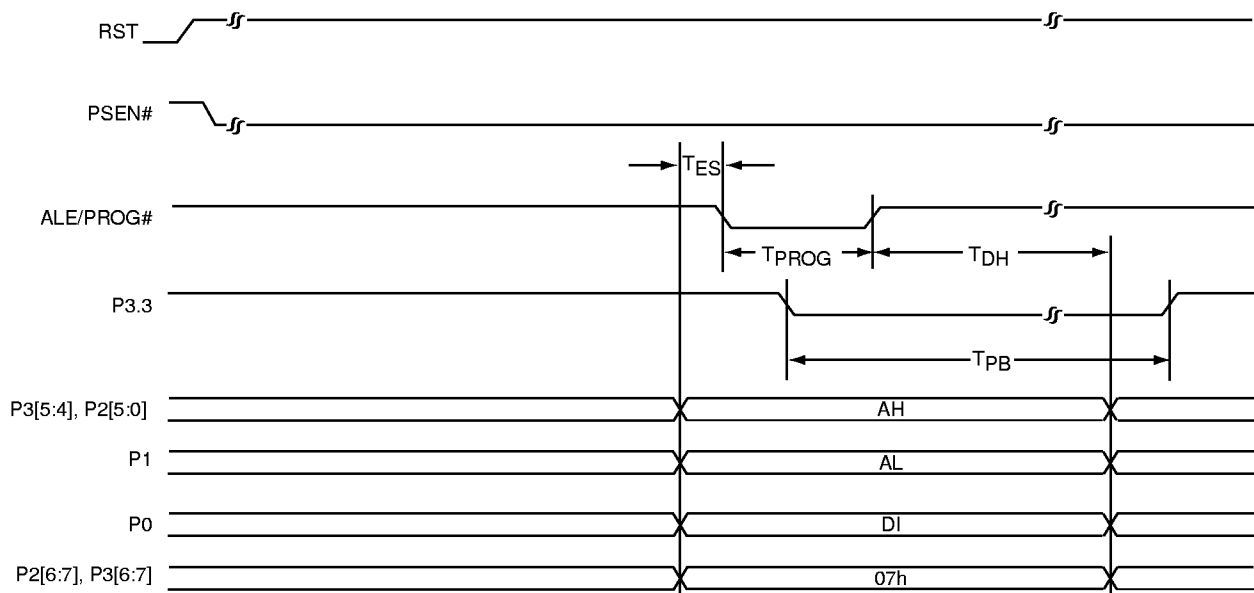
Erase one of the flash memory blocks, if the security lock is not activated on that flash memory block. The highest address bit (A15) determines which block is erased. For example, if A15 is "0", primary flash memory block is erased.



325 ILL F05.10

FIGURE 15: SECTOR ERASE

Erase the addressed sector if the security lock is not activated on that flash memory block.



325 ILL F06.11

FIGURE 16: BYTE PROGRAM

Program the addressed code byte if the byte location has been successfully erased and not yet programmed. This operation is only allowed when the security lock is not activated on that flash memory block.



FlashFlex51 MCU

SST89C54 / SST89C58 / SST89C59

Advance Information

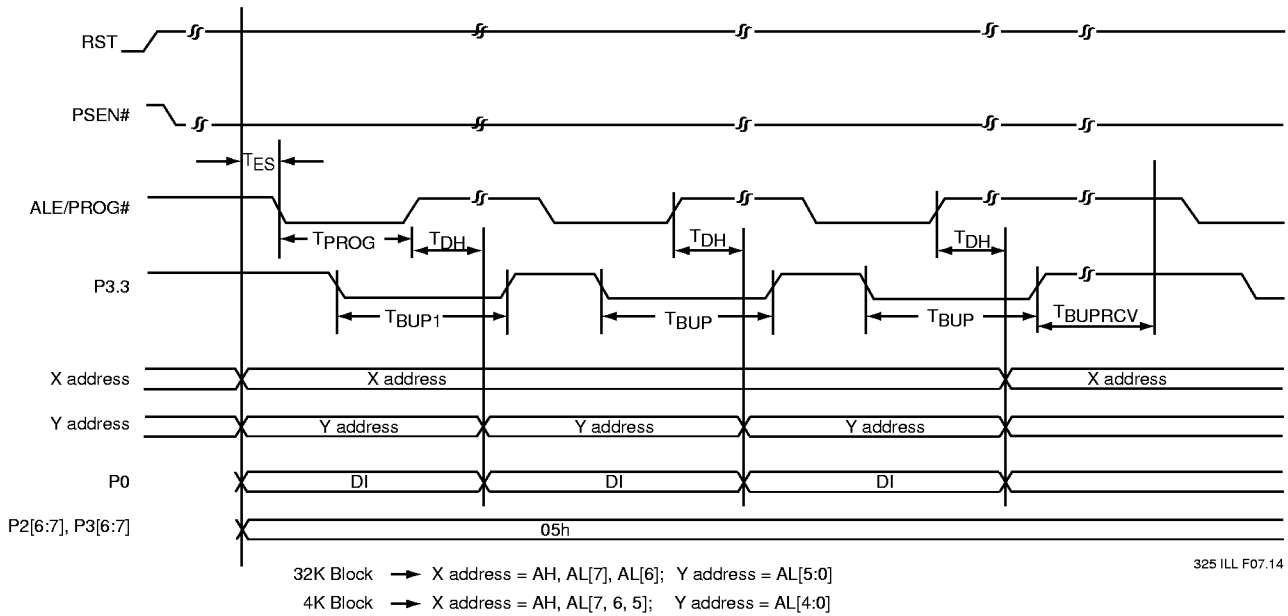


FIGURE 17: BURST PROGRAM

Program the entire addressed row by burst programming each byte sequentially within the row if the byte location has been successfully erased and not yet programmed. This operation is only allowed when the security lock is not activated on that flash memory block.

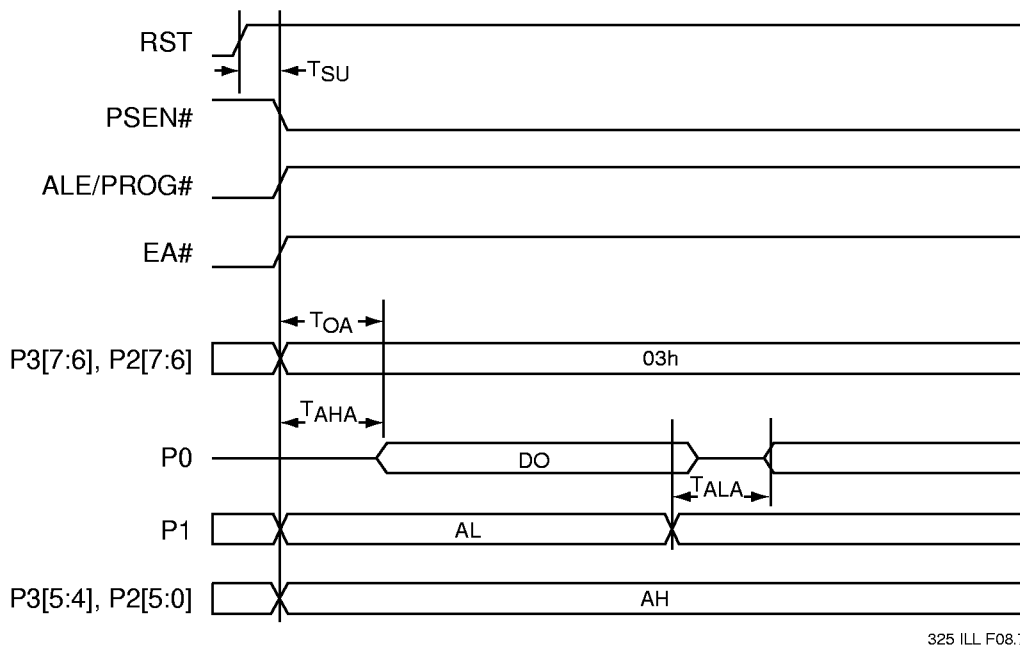


FIGURE 18: VERIFY BYTE

Read the code byte from the addressed flash memory location if the security lock is not activated on that flash memory block.



IN-APPLICATION PROGRAMMING MODE

The SST89C54/58/59 offers 20/36/68 KByte of in-application re-programmable flash memory. During In-Application Programming, the CPU of the microcontroller enters IAP Mode. The two blocks of flash memory allows the CPU to concurrently execute user code from one block, while the other is being reprogrammed. The CPU may also fetch code from an external memory while all internal flash is being reprogrammed. The chip can start the In-Application Programming operation either with the external program code execution being enabled (EA# = L) or disabled (EA#=H). The mailbox registers (SFCM, SFAL, SFAH, SFDT and SFCF) located in the Special Function Register (SFR), control and monitor the device's erase and program process.

There are six (6) IAP commands plus a setup command, which can be issued via the command mailbox register, SFCM at SFR location B2h. A pair of mailbox register addresses the memory array of the SuperFlash blocks: SFAL, low order address at SFR location B3h, and SFAH, the high order address at SFR location B4h. Data is buffered through the SFDT register at SFR location B5h. SFCF, the configuration register at SFR location B6h, provides security lock status program counter and visibility to the secondary flash memory block. The list in Table 6 outlines all the commands and their associated bit settings of the mailbox registers.

In-Application Programming Mode Clock Source

During IAP Mode, both the CPU core and the flash controller unit run off the external clock input. However, an internal oscillator will provide timing references for Program and Erase operations. In fact, the timing of Program and Erase operations will be identical between External Host Mode and In-Application Mode. The internal oscillator is only turned on when required, it is turned off as soon as the Flash operation completes.

Setup Command

The Setup Command provides additional protection against code corruption of the SuperFlash memory. A Setup Command byte, 5Dh or DDh, must be programmed into the SFCM register prior to issuing each of the IAP Mode command, otherwise, the IAP Mode commands will be ignored. The Setup Command is required for each individual IAP Command (except VERIFY BYTE) and is canceled after an execution of the IAP command. The Setup Command must be reinitialized when the system resets, including Watchdog timeout, or when the device exits from an idle or power down mode.

In-Application Programming Mode Commands

All of the following commands can only be initiated in the IAP Mode. In all situations, writing the control byte to the (SFCM) register will initiate all of the operations. All commands (except CHIP ERASE) will not be enabled if the Security Byte is set and security features are enabled on the selected memory block. The critical timing for all Erase and Program commands, is self-generated by the Flash memory controller on-chip.

The two Program commands are for programming new data into the memory array. The portion of the memory array to be programmed should be in the erased state, FFh. If the memory is not erased, then erase it with the appropriate Erase command. Warning: do not write (program or erase) to a block that the code is currently fetching from. This can "hang" the CPU and may even corrupt program data as it is being executed.

The CHIP ERASE command erases all bytes in both memory blocks (16/32/64K and 4K). This command ignores the Security Lock status and will erase the Security Byte and Re-Map Byte. The CHIP ERASE command is initiated as follows:

- 1.) Move 55h to the SuperFlash Data Register (SFDT) (i.e. "MOV SFDT, #55h" where SFDT is the register address). This serves as a dual level precautionary measure to prevent accidental chip erasure.
- 2.) Move 5Dh or DDh to the SuperFlash Command Register (SFCM) (i.e., "MOV SFCM, #5Dh or MOV SFCM, #0DDh"). This is a "setup command" sequence prior to Program and Erase operations to prevent inadvertent program or erase within the SuperFlash memory.
- 3.) Move the termination mode FIE and Chip Erase command FCM to the SuperFlash Command Register (SFCM) (i.e. MOV SFCM, #87h or MOV SFCM, #07h). If FIE is set, INT1# will interrupt the system when the erase is complete. Otherwise you must poll the system to determine when the erase is complete.



FlashFlex51 MCU

SST89C54 / SST89C58 / SST89C59

Advance Information

The BLOCK ERASE command erases all bytes in one of the two memory blocks (16/32/64K or 4K). The selection of the memory block to be erased is determined by the "A15" bit (SFAH[7]) of the SuperFlash Address Register. If (SFAH[7]) is a "0", the primary flash memory block is selected (16/32/64K). If (SFAH[7]) is a "1", the secondary flash memory block is selected (4K). The BLOCK ERASE command is initiated as follows:

- 1.) Move the block address to (SFAH) (i.e. MOV SFAH, #80h or MOV SFAH, #00h).
- 2.) Move 55h to the SuperFlash Data Register (SFDT) (i.e. "MOV SFDT, #55h" where SFDT is the register address). This serves as a dual level precautionary measure to prevent accidental erasure.
- 3.) Move 5Dh or DDh to the SuperFlash Command Register (SFCM) (i.e., "MOV SFCM, #5Dh or MOV SFCM, #0DDh"). This is an "setup command" sequence prior to Program and Erase operations to prevent inadvertent program or erase within the SuperFlash memory.
- 4.) Move the termination mode FIE and Block Erase command FCM to (SFCM) (i.e. MOV SFCM, #8Fh or MOV SFCM, #0Fh). If FIE is set, INT1# will interrupt the system when the erase is complete. Otherwise you must poll the SFCF[3] register to determine when the erase is complete.

The SECTOR ERASE command erases all of the bytes in a sector. The sector size for the primary flash memory (Address buffer locations 0-3FFFh/7FFFh/FFFFh) is 128 bytes. The sector size for the secondary flash memory (Address buffer locations F000h-FFFFh) is 64 bytes. The SECTOR ERASE command is initiated as follows:

- 1.) Move the sector address to (SFAH) and to (SFAL).
- 2.) Move 5Dh or DDh to the SuperFlash Command Register (SFCM) (i.e., "MOV SFCM, #5Dh or MOV SFCM, #0DDh"). This is an "setup command" sequence prior to Program and Erase operations to prevent inadvertent program or erase within the SuperFlash memory.
- 3.) Move the termination mode FIE and Sector Erase command FCM to (SFCM) (i.e. MOV SFCM, #8Bh or MOV SFCM, #0Bh). If FIE is set, INT1# will interrupt the system when the erase is complete. Otherwise you must poll the SFCF[3] register to determine when the erase is complete.

The BYTE PROGRAM command programs data into a single byte. The BYTE PROGRAM command is initiated as follows:

- 1.) Move the high order address byte AH to (SFAH).
- 2.) Move the low order address byte AL to (SFAL).
- 3.) Move the data to the (SFDT).

- 4.) Move 5Dh or DDh to the SuperFlash Command Register (SFCM) (i.e., "MOV SFCM, #5Dh or MOV SFCM, #0DDh"). This is an "setup command" sequence prior to Program and Erase operations to prevent inadvertent program or erase within the SuperFlash memory.
- 5.) Move the termination mode FIE and Byte Program command FCM to (SFCM) (i.e. MOV SFCM, #8Eh or MOV SFCM, #0Eh). If FIE is set, INT1# will interrupt the system when the program is complete. Otherwise you must poll the SFCF[3] register to determine when the program is complete.

The BURST PROGRAM command programs data to an entire row, sequentially byte by byte. The BURST PROGRAM command is initiated as follows:

- 1.) Move the high order address byte to (SFAH).
- 2.) Move the low order address byte to (SFAL).
- 3.) Move the data to (SFDT).
- 4.) Move 5Dh or DDh to the SuperFlash Command Register (SFCM) (i.e., "MOV SFCM, #5Dh or MOV SFCM, #0DDh"). This is an "setup command" sequence prior to Program and Erase operations to prevent inadvertent program or erase within the SuperFlash memory.
- 5.) Move the termination mode FIE and Burst Program command FCM to (SFCM) (i.e. MOV SFCM, #8Ah or MOV SFCM, #0Ah). If FIE is set, INT1# will interrupt the system when the program is complete. Otherwise you must poll the SFCF[3] register to determine when the program is complete.
- 6.) Wait for interrupt or poll for end of burst.
- 7.) If another Burst Program is needed return to step 4 (same row).

The VERIFY BYTE command allows the user to verify that the SST89C54/58/59 has correctly performed an Erase or Program command. The VERIFY BYTE command is initiated as follows:

- 1.) Move the high order address byte AH to (SFAH).
- 2.) Move the low order address byte AL to (SFAL).
- 3.) Move the termination mode FIE and Verify Byte command FCM to (SFCM) (i.e. MOV SFCM, #8Ch or MOV SFCM, #0Ch).

Polling

A command that uses the polling method to signify the completion of an operation must check the BUSY bit (SFCF[3]). Copy the (SFCF) register into temporary memory and mask bit 3. Once it is isolated, the status of the BUSY bit can be checked.

MOVC instruction may also be used for verification of the Programming and Erase operation of the flash memory.



TABLE 6: IN-APPLICATION PROGRAMMING MODE COMMANDS

Operation	SFAH [7:0]	SFAL [7:0]	SFDT [7:0]	SFCM ¹ [7:0]	SFCM ² [7:0]
CHIP ERASE	X	X	55h	5Dh/DDh	87h/07h
BLOCK ERASE	80h/00h	X	55h	5Dh/DDh	8Fh/0Fh
SECTOR ERASE	AH	AL	X	5Dh/DDh	8Bh/0Bh
BYTE PROGRAM	AH	AL	DI	5Dh/DDh	8Eh/0Eh
BURST PROGRAM	AH	AL	DI	5Dh/DDh	8Ah/0Ah
VERIFY (Read) BYTE	AH	AL	DO	–	8Ch/0Ch

325 PGM T5.12

Notes: X = Don't care; AL = Address low order byte; AH = Address high order byte;
DI = Data Input; DO = Data Output

1. The value 5Dh or DDh for SFCM is needed before performing any Program and Erase operations. It serves as an "setup command" sequence
2. SFCM(7:0) 8X/0X = Interrupt/Polling Enable for flash operation completion

TABLE 7: FLASH MEMORY PROGRAMMING/VERIFICATION PARAMETERS ($T_J = 0^\circ\text{C}$ TO $+125^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$, $V_{SS} = 0V$)

Parameter (1, 2, 4, 5)	Symbol	Min.	Max.	Unit
Reset Setup Time	T_{SU}	3		μs
Read ID Command Setup Time	T_S	0		ns
Read ID Command Width (3)	T_{RD}	250		ns
PSEN# Setup Time	T_{ES}	250		ns
Chip Erase Time	T_{CE}	4.25		ms
Block Erase Time	T_{BE}	4.25		ms
Sector Erase Time	T_{SE}	1.1		ms
Program Setup Time	T_{PROG}	1.2		μs
Byte Program Time (6)	T_{PB}		97	μs
Verify Command Setup time	T_{OA}	35		ns
Verify High Order Address Setup Time	T_{AHA}	35		ns
Verify Low Order Address Setup Time	T_{ALA}	35		ns
Burst Program (6,7)	T_{BUP}	31	51	μs
Burst Program Recovery	T_{BUPRCV}		35	μs

325 PGM T4.14

Note:

1. All timing numbers are pre-simulation and subject to change before silicon verification.
2. All signals that align together in the timing diagrams should be derived from the same clock edge. Set up and hold times are not critical if they are within 10ns.
3. Reading operation is combinatorial. Sequence of timing edges are not important. The latest valid signal determines the access time.
4. All timing measurements are from the 50% of the input to 50% of the output.
5. All input waveforms have rise and fall time of 1ns.
6. Don't Program (write "0") any byte twice before next erase.
7. Timing is based on 126ns clock cycles.



FlashFlex51 MCU

SST89C54 / SST89C58 / SST89C59

Advance Information

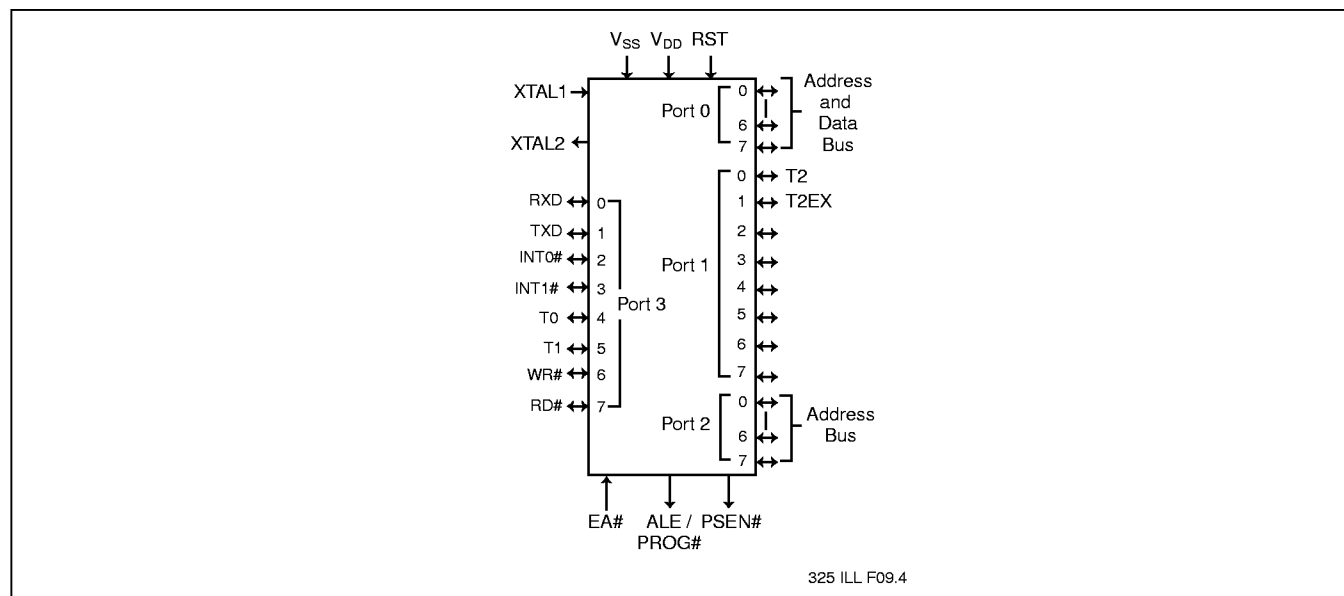


FIGURE 19: IN-APPLICATION PROGRAMMING MODE I/O ASSIGNMENT

TIMERS/COUNTERS

The SST89C54/58/59 have three 16-bit registers that can be used as either timers or event counters. The three Timers/Counters are the Timer 0 (T0), Timer 1 (T1), and Timer 2 (T2) registers. These three registers are located in the SFR as pairs of 8-bit registers. The low byte of the T0 register is stored in the Timer 0 LSB (TL0) special function register and the high byte of the T0 register is stored in the Timer 0 MSB (TH0) special function register. The low byte of the T1 register is stored in the Timer LSB (TL1) special function register and the high byte of the T1 register is stored in the Timer 1 MSB (TH1) special function register. The low byte of the T2 register is stored in the Timer 2 LSB (TL2) special function register and the high byte of the T2 register is stored in the Timer 2 MSB (TH2) special function register.

SERIAL I/O (UART)

The SST89C54/58/59 Serial I/O ports is a full duplex port that allows data to be transmitted and received simultaneously in hardware by the transmit and receive registers, respectively, while the software is performing other tasks. The Serial I/O port performs the function of an UART (Universal Asynchronous Receiver/Transmitter) chip. The transmit and receive registers are both located in the Serial Data Buffer (SBUF special function register. Writing to the SBUF register loads the transmit register, and reading from the SBUF register obtains the contents of the receive registers.

The Serial I/O port has four modes of operation which are selected by the Serial Port Mode Specifier (SM0 and SM1) bits of the Serial Port Control (SCON) special function register. In all four modes, transmission is initiated by any instruction that uses the SBUF register as a destination register. Reception is initiated in mode 0 when the Receive Interrupt (RI) flag bit of the Serial Port Control (SCON) special function register is cleared and the Reception Enable/ Disable (REN) bit of the SCON register is set. Reception is initiated in the other modes by the incoming start bit if the REN bit of the SCON register is set.



INTERRUPT

The SST89C54/58/59 provide 6 interrupt sources, which include two external interrupts (INT0# and INT1#), three Timer/Counter Interrupts (TF0, TF1, and TF2), and one from the serial port (SI or TI). The Interrupt Enable (IE) special function register is the source of the interrupts. Each of the bits that generate the interrupts may be set or cleared by software with the same result as setting or clearing the bits through hardware. Therefore, interrupts may be generated or canceled by software. Also, interrupts can be enabled or disabled by setting or clearing individual bits of the IE register. The SST89C54/58/59 also contain a global enable bit which allows all of the interrupts to be enabled or disabled by setting or clearing the EA bit of the IE register. Please refer to the SST89C54/58/59 User's Manual for a more detailed description of the Interrupt System.

Interrupt Priority Levels

Individual interrupts can be programmed as a low-priority or a high-priority interrupt by setting or clearing the corresponding bit in the Interrupt Priority (IP) special function register. A 0 value is designated a low priority and a 1 value is the high priority. Please refer to the SST89C54/58/59 User's Manual for a more vivid description about Interrupt Priority Levels.

WATCHDOG TIMER

The SST89C54/58/59 offer an enhanced programmable watchdog timer for fail safe protection against software "hang" and allows an automatic recovery from such software upset.

To protect the system against software "hang", the user's program has to refresh the watchdog timer within a previously programmed time period. If the software fails to do this periodical refresh, an internal hardware reset will be initiated. The software can be designed such that the watchdog times out if the program does not work properly. It also times out if a software error is based on the hardware related problems.

The watchdog timer in the SST89C54/58/59 share the same time base with the flash controller unit. When the flash controller unit is operating, the time base will be re-started by the hardware periodically, hence elongate the time-out period of the watchdog timer. The higher most 8-bits of the time base register are used as the reload register of the watchdog timer.

Figure 20 provides a block diagram of the Watchdog Timer. Two SFRs (WDTC and WDTD) control watchdog timer operation. During idle mode, WDT operation is temporarily suspended, and resumes upon an interrupt exit from idle.

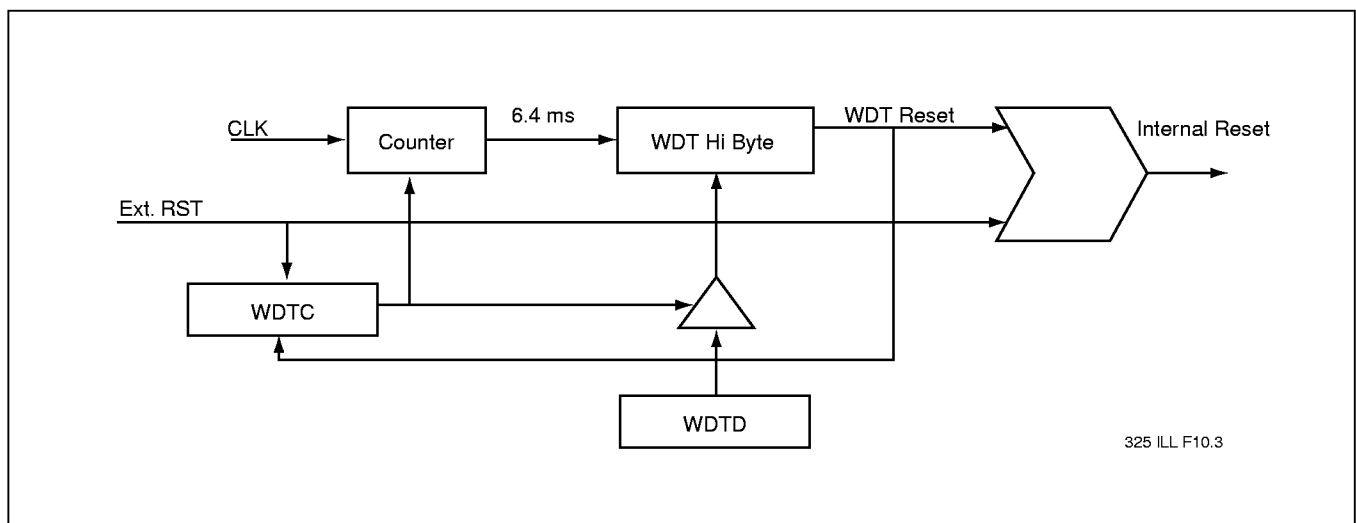


FIGURE 20: BLOCK DIAGRAM OF PROGRAMMABLE WATCHDOG TIMER



FlashFlex51 MCU

SST89C54 / SST89C58 / SST89C59

Advance Information

SECURITY LOCK

The Security feature protects against software piracy and prevents the contents of the flash from being read by unauthorized parties. It also protects against code corruption resulting from accidental erasing and programming to the internal flash memory locations. The security bits are located in the highest address location, FFFFh, of the SST89C54/58/59 program memory space. Only bits [3:0] are used for security coding, bits [6:4] are reserved, and bit [7] is used to enable "Interrupt Re-mapping (REMC)". Refer to the Memory Organization section for details on flash memory re-mapping.

When the security lock is activated, the MOVc instructions executed from external program memory or unlocked flash memory are disabled from fetching code bytes from locked memory blocks (See Table 8). The security lock can either "hard" lock both flash memory blocks or just "hard" lock the secondary flash memory block (Block 1) independently. When the memory blocks are locked, the following commands are not allowed on the locked flash memory blocks:

- SECTOR ERASE
- BLOCK ERASE
- PROGRAM BYTE
- BURST PROGRAM
- VERIFY BYTE

Both memory blocks may be "soft" locked, allowing In-Application Programming. This feature allows the device to enter IAP Mode executing from internal memory, but inhibits the device from entering IAP Mode executing from external memory or External Host Mode. Table 9 lists the security lock options and commands allowed for each option.

ACTIVATION AND DEACTIVATION OF THE SECURITY LOCK

For both External Host and In-Application Programming modes, the security bits, XXXXBBBB¹, XXXX0101b (X5h) or XXXX0011b (X3h), must first be programmed into the address location FFFFh using the BYTE or BURST PROGRAM operation. Bits [3:2] are used to define lock states of Block 1 (4K block) and bit [1:0] are used to define lock states of Block 0 (32K block). After the security bits has been programmed into address location FFFFh, the security lock is activated following a successful system reset.

To deactivate the security lock, the security byte at location FFFFh is programmed with a value of, XXXX1111b (XFh), via the CHIP ERASE operation. The default value of the security byte is XFh.

TABLE 8: INTERNAL AND EXTERNAL PROGRAM MEMORY ACCESS WITH SECURITY LOCK ACTIVATED

MOVc INSTRUCTIONS EXECUTED FROM	ACCESS TO LOCKED PROGRAM MEMORY	ACCESS TO UNLOCKED OR EXTERNAL PROGRAM MEMORY
locked program memory	YES	YES
unlocked or external program memory	NO	YES

TABLE 9: SECURITY LOCK OPTIONS

Security Bits	SFCF [6:5]	EA#	blk Sel	Block Erase	Sector Erase	Byte Program	Burst Program	Verify Byte	Description
XXXX1111b	00	X	X	Y	Y	Y	Y	Y	no lock, (default)
XXXXBBBB ¹	11	X	X	N	N	N	N	N	both blocks locked
XXXX0011b	01	X	0	Y	Y	Y	Y	Y	only block 1 (4KB) is locked
		X	1	N	N	N	N	N	
XXXX0101b	10	0	0/1	N	N	N	N	N	both blocks are accessible only through In-Application Programming
		1	0/1	Y	Y	Y	Y	Y	

325 PGM T6.9

Note: **Security Bits** = Value of Security Bits [3:0] at location FFFFh; **SFCF[6:5]** = Bit 5 and 6 of SFCF register are read only bits; **EA#** = Ext. Access enable input pin: 1 – running code from internal memory, 0 – running code from external enable; **blkSel** = Block Select signal (internal): 1 – block 1 (4Kx8), 0 – block 0 (32Kx8); **X** = don't care; **Y** = command allowed; **N** = command not allowed.

SFCF [6:5] represents the Security Lock Decoding bits of the SuperFlash Configuration (SFCF) special function register and they are read only bits. The bits are only updated out of reset, i.e. dynamic changes to address location FFFFh is not tracked until a reset cycle, with the exception that SFCF [6:5] are cleared upon successful completion of a CHIP ERASE

¹ XXXXBBBB – B denotes any combination of binary values that do not unlock or partially lock the device.



In-Application Programming Mode

The security locks option, XXXX0101b, “soft” locks both flash memory blocks. This lock option allows the user to update the code in the locked flash memory blocks under a pre-determined secure environment. When both flash memory blocks are “soft” locked, the software code executing from one internal flash memory block can perform In-Application Programming on the other block. In other words, code residing in Block 1 may program to Block 0 and vice versa. The following IAP Mode commands issued through the command mailbox register, SFCM, and executed from the internal program memory can be operated on both Block 0 and Block 1: BLOCK ERASE, SECTOR ERASE, BYTE PROGRAM, BURST PROGRAM and VERIFY BYTE.

The security bits, XXXXBBBBb (both blocks “hard” locked), prohibits In-Application Programming (IAP) to the flash memory blocks. (XXXXBBBBb – B denotes any combination of binary values that does not unlock or partially lock the device). Only the CHIP ERASE operation will erase both blocks including the security bits. If the security bits, XXXX0011b (only Block 1 is locked), In-Application Programming is only allowed in Block 0.

A CHIP ERASE operation can deactivate, or change the level of, the security lock after it is set. CHIP ERASE will set the security byte to the value of XFh. The In-Application Programming operation with program code execution from either internal flash memory or external program code storage can write a new lock option to the security bits, and the new security lock will activate on the next system reset.

External Host Mode

If the security lock is activated, the following External Host Mode commands are not allowed on the locked flash memory blocks: SECTOR ERASE, BLOCK ERASE, BYTE PROGRAM, BURST PROGRAM, and VERIFY BYTE. Only the CHIP ERASE operation can deactivate, or change level of, the security lock after it is set. CHIP ERASE will set the security bits to the value of XXXX1111b.

RESET

A system reset initializes the MCU and begins program execution at program memory location 0000h. The reset input for the SST89C54/58/59 is the RST pin. In order to reset the SST89C54/58/59, a logic level high must be applied to the RST pin for at least two machine cycles (24 clocks), after the oscillator becomes stable. ALE, PSEN# are weakly pulled high during reset. During reset, ALE and PSEN# output a high level in order to perform correct reset. This level must not be affected by external element. A system reset will not affect the 256 bytes of on-chip RAM while the SST89C54/58/59 is running, however, the contents of the on-chip RAM during power up are indeterminate. All Special Function Registers (SFR) return to their reset values, which are outlined in Tables 3A to 3E.

Power-On Reset

At initial power up, the port pins will be in a random state until the oscillator has started and the internal reset algorithm has written one’s to all the pins. Powering up the device without a valid reset could cause the CPU to start executing instructions from an indeterminate location. Such undefined states may inadvertently corrupt the code in the flash.

To ensure a good power-on reset, it is required that the V_{DD} rise time does not exceed 1 ms and the oscillator start up time does not exceed 10 ms. Figure 22 shows the maximum delay time allowed between initial power up and reset. V_{DD} should lag no more than 10 ns behind RST at voltages above 1.4 V. A common method to extend the RST signal is to implement a RC circuit by connecting the RST pin to V_{DD} through a 10 μF capacitor and to V_{SS} through an 8.2K resistor as shown in Figure 21. This method maintains the necessary relationship between V_{DD} and RST to avoid programming at an indeterminate location, which may cause code corruption in the flash.

In addition to the external Power-On Reset circuit, the SST89C54/58/59 have an internal fail-safe mechanism that protects the flash during a Power-On Reset or during a Brown-Out condition. The internal Power-On Reset/ Brown-Out circuit further prevents inadvertent information to be programmed to the flash. It should be noted that the internal Power-On Reset/ Brown-Out protection circuit only provides additional protection for the flash, an external circuit is still necessary to ensure both the flash and the CPU resets properly.

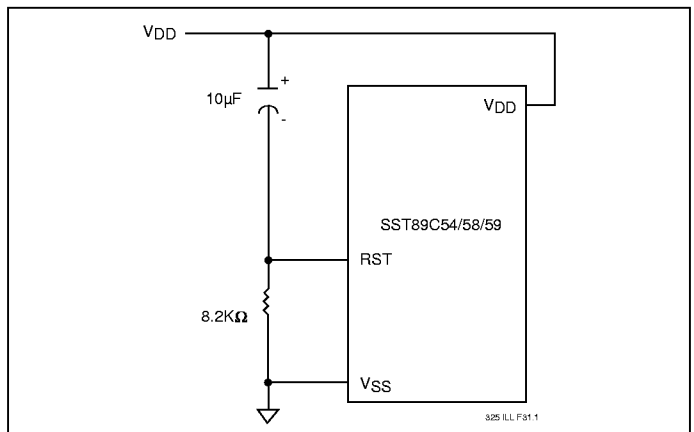


FIGURE 21: POWER-ON RESET CIRCUIT

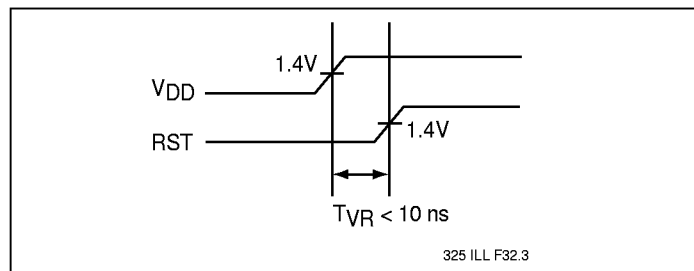


FIGURE 22: MINIMUM V_{DD} TO RST FOR POWER-ON RESET



FlashFlex51 MCU

SST89C54 / SST89C58 / SST89C59

Advance Information

POWER-SAVING MODES

The FlashFlex51 Family of MCUs provide three power-saving modes of operation for applications where power consumption is critical. The three power-saving modes are Idle, Power Down and Standby (Stop Clock) modes. In the Idle mode, the current drain is approximately 25% of the current drain when the device is fully active, and the clock signal is gated off to the MCU, but remains operating to all other functions within the device (e.g., inter-

rupts, timers and serial port). Idle mode is initiated by software. The Power Down and Standby (Stop Clock) modes are similar, both reduce device current drain to approximately 15 microamperes. However, entry to the two modes is different, Power Down mode is entered by software, while Standby (Stop Clock) mode is controlled by hardware (gating on and off the system clock). Table 10 below outlines the different power-saving modes, indicating entry and exit procedures and functionality within the MCU during the power-saving modes.

TABLE 10: FLASHFLEX51 POWER SAVING MODES

Mode	Initiated by	Current Drain	State of MCU	Exited by
Idle Mode	Software (Set IDL bit in PCON)	25% of I_{DD} level when device is fully active	CLK running. Interrupts, serial port and timers/counters continue to be clocked, but the MCU clock is gated off. ALE and PSEN# sigs at a HIGH level during Idle. All registers remain unchanged.	Enabled interrupt or hardware reset. Start of <u>interrupt</u> clears IDL bit and exits Idle mode, and after the ISR RETI instruction, the program resumes normal processing (note 1). A hardware reset starts the device similar to power-on reset. (See note 2.)
Power Down Mode	Software (Set PD bit in PCON)	Approximately 15 microamps. And V_{DD} can be reduced by ext. hardware to 2V during (after entry and before exit) power down mode.	CLK gated Off to MCU, serial port, timer/counters and internal interrupts. On-chip SRAM and SFR data is maintained. ALE and PSEN# signals at a LOW level during Power Down.	External interrupt or hardware reset. From <u>external</u> interrupt, on-chip RAM and SFRs retain their data. Once the ISR ends, normal processing (note 1) resumes. A hardware <u>reset</u> starts the device similar to power-on reset.
Standby (Stop Clock) Mode	External hardware gates OFF the external clock input to the MCU. This gating shall be synchronized with an input clock transition (low-to-high or high-to-low).	Approximately 15 microamps. And V_{DD} can be reduced by ext. hardware to 2V during (after entry and before exit) power down mode.	Internal state of the MCU is totally preserved.	Gate ON external clock, and begin executing at <u>next clock</u> in normal processing.

325 PGM T8.2

- Notes:**
1. Normal processing refers to program execution beginning at the instruction following the one that invoked this particular power reduction mode.
 2. When the idle mode is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. If needed in a specific application, a user could consider placing two or three NOP instructions after the instructions that invoke idle mode to eliminate any problems



CLOCK INPUT OPTIONS

Shown in Figure 23 are the input and output of an inverter amplifier, which can be configured for use as an on-chip oscillator.

When driving the device from an external clock source, XTAL2 should be left disconnected and XTAL1 should be driven. The internal clocking circuitry is through a flip-flop (divide-by-two). Minimum and maximum high and

low times specified on the data sheet must be observed, but there are no requirements on the duty cycle of the external clock signal.

At start-up, the external oscillator may encounter up to a 100 pF load at XTAL1 due to interaction between the amplifier and its feedback capacitance. However, the capacitance will not exceed 20 pF once the external signal meets the V_{IL} and V_{IH} specifications.

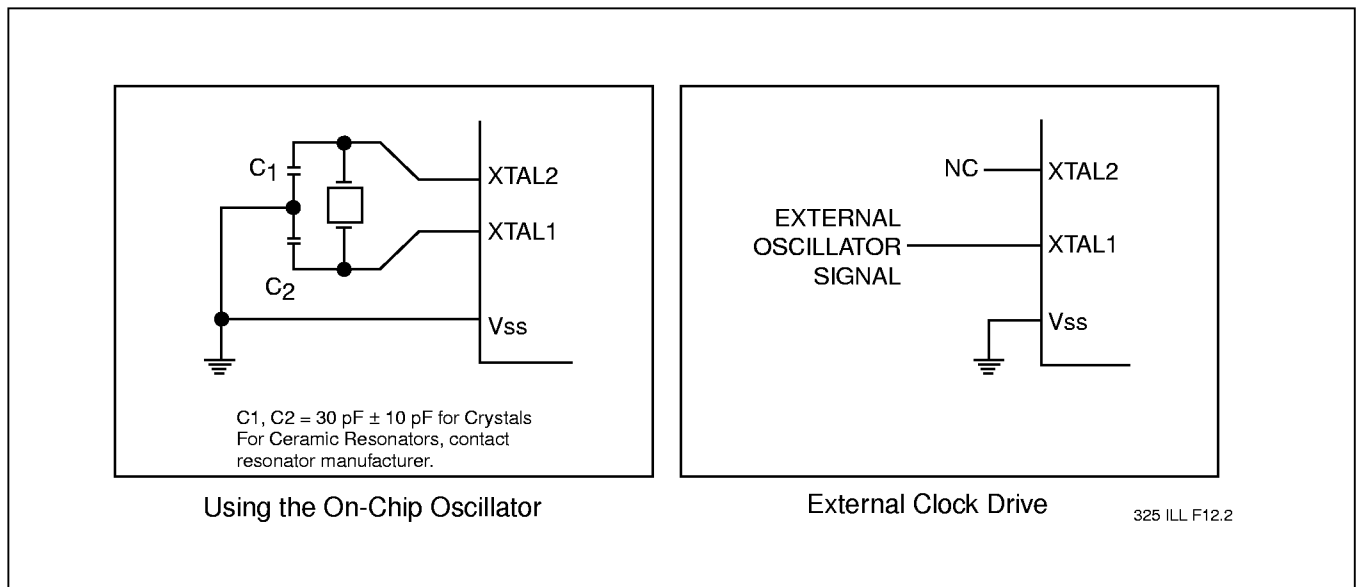


FIGURE 23: OSCILLATOR CHARACTERISTICS



FlashFlex51 MCU

SST89C54 / SST89C58 / SST89C59

Advance Information

ELECTRICAL SPECIFICATION

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under “Absolute Maximum Stress Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Ambient Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to + 150°C
Voltage on EA# Pin to V _{SS}	-0.5V to +14.0V
Transient Voltage (<20ns) on Any Other Pin to V _{SS}	-1.0V to +6.5V
Maximum I _{OL} per I/O Pin	15 mA
Package Power Dissipation Capability (T _A = 25°C)	1.5W
Through Hole Lead Soldering Temperature (10 Seconds)	300°C
Surface Mount Lead Soldering Temperature (3 Seconds)	240°C
Output Short Circuit Current ⁽¹⁾	100 mA

Note ⁽¹⁾ Outputs shorted for no more than one second. No more than one output shorted at a time.
(Based on package heat transfer limitations, not device power consumption.)

NOTICE: This specification contains preliminary information on new products in production. The specifications are subject to change without notice.

Operation Range

TABLE 11: OPERATING RANGE

Symbol	Description	Min.	Max	Unit
T _A	Ambient Temperature Under Bias			
	Standard	0	+70	°C
	Industrial	-40	+85	°C
V _{DD}	Supply Voltage	2.7	5.5	V
f _{OSC}	Oscillator Frequency	0	33	MHz
	For In-Application Programming	0.25	33	MHz

325 PGM T10.1

TABLE 12: RELIABILITY CHARACTERISTICS

Symbol	Parameter	Minimum Specification	Units	Test Method
N _{END}	Endurance	10,000	Cycles	JEDEC Standard A117
T _{DR} ⁽¹⁾	Data Retention	100	Years	JEDEC Standard A103
V _{ZAP_HBM} ⁽¹⁾	ESD Susceptibility Human Body Model	2000	Volts	JEDEC Standard A114
V _{ZAP_MM} ⁽¹⁾	ESD Susceptibility Machine Model	300	Volts	JEDEC Standard A115
I _{LTH} ⁽¹⁾	Latch Up	100+I _{DD}	mA	JEDEC Standard 78

Note: ⁽¹⁾This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

325 PGM T11.1



TABLE 13A: DC ELECTRICAL CHARACTERISTICS

T_{AMB} = 0°C TO + 70°C OR -40°C TO +85°C, 33MHz DEVICES; 5V ±10%; V_{SS} = 0V

Symbol	Parameter	Test Conditions	Limits		Units
			Min	Max	
V _{IL}	Input Low Voltage	4.5 < V _{DD} < 5.5	-0.5	0.2V _{DD} - 0.1	V
V _{IH}	Input High Voltage (ports 0,1,2,3)	4.5 < V _{DD} < 5.5	0.2 V _{DD} + 0.9	V _{DD} + 0.5	V
V _{IH1}	Input High Voltage (XTAL1, RST)	4.5 < V _{DD} < 5.5	0.7 V _{DD}	V _{DD} + 0.5	V
V _{OL}	Output Low Voltage (Ports 1.5, 1.6, 1.7)	V _{DD} = 4.5 V I _{OL} = 16 mA		1.0	V
V _{OL}	Output Low Voltage (Ports 1, 2, 3) ⁵	V _{DD} = 4.5 V I _{OL} = 100 μA ¹ I _{OL} = 1.6 mA ¹ I _{OL} = 3.5 mA ¹		0.3	V
				0.45	V
				1.0	V
V _{OL1}	Output Low Voltage (Port 0, ALE, PSEN#) ^{4,5}	V _{DD} = 4.5 V I _{OL} = 200 μA ¹ I _{OL} = 3.2 mA ¹		0.3	V
				0.45	V
V _{OH}	Output High Voltage (Ports 1, 2, 3, ALE, PSEN#) ²	V _{DD} = 4.5 V I _{OH} = -10 μA I _{OH} = -30 μA I _{OH} = -60 μA	V _{DD} - 0.3		V
			V _{DD} - 0.7		V
			V _{DD} - 1.5		V
V _{OH1}	Output High Voltage (Port 0 in External Bus Mode) ²	V _{DD} = 4.5 V I _{OH} = -200 μA I _{OH} = -3.2 mA	V _{DD} - 0.3		V
			V _{DD} - 0.7		V
I _{IL}	Logical 0 Input Current (Ports 1, 2, 3)	V _{IN} = 0.4V	-1	-75	μA
I _{TL}	Logical 1-to-0 Transition Current (Ports 1, 2, 3) ³	V _{IN} = 2V		-650	μA
I _{LI}	Input Leakage Current (Port 0)	0.45 < V _{IN} < V _{DD} -0.3		±10	μA
R _{RST}	RST Pulldown Resistor		40	225	kΩ
C _{IO}	Pin Capacitance ⁶	@ 1 MHz, 25°C		15	pF
I _{DD}	Power Supply Current ⁷ In-Application Mode	V _{DD} = 5V		70	mA
			@ 12 MHz		88
	@ 33 MHz				
	Active Mode				
	@ 12 MHz			25	mA
	@ 33 MHz			45	mA
	Idle Mode				
	@ 12 MHz			9.5	mA
	@ 33 MHz			15.5	MA
	Standby (Stop Clock) Mode		T _{amb} = 0°C to + 70°C	100	μA
	T _{amb} = -40°C to +85°C	125	μA		
Power Down Mode	V _{DD} = 2V				
	T _{amb} = 0°C to + 70°C	40	μA		
	T _{amb} = -40°C to +85°C	50	μA		

325 PGM T12A.3



FlashFlex51 MCU

SST89C54 / SST89C58 / SST89C59

Advance Information

TABLE 13B: DC ELECTRICAL CHARACTERISTICS

T_{AMB} = 0°C TO +70°C OR -40°C TO +85°C, 12 MHz DEVICES; 3V ±10%; V_{SS} = 0V

Symbol	Parameter	Test Conditions	Limits		Units
			Min	Max	
V _{IL}	Input Low Voltage	2.7 < V _{DD} < 3.3	-0.5	0.7	V
V _{IH}	Input High Voltage (ports 0,1,2,3)	2.7 < V _{DD} < 3.3	0.2 V _{DD} + 0.9	V _{DD} + 0.5	V
V _{IH1}	Input High Voltage (XTAL1, RST)	2.7 < V _{DD} < 3.3	0.7 V _{DD}	V _{DD} + 0.5	V
V _{OL}	Output Low Voltage (Ports 1.5, 1.6, 1.7)	V _{DD} = 2.7 V I _{OL} = 16 mA		1.0	V
V _{OL}	Output Low Voltage (Ports 1, 2, 3) ⁵	V _{DD} = 2.7 V I _{OL} = 100 μA ¹		0.3	V
		I _{OL} = 1.6 mA ¹		0.45	V
		I _{OL} = 3.5 mA ¹		1.0	V
V _{OL1}	Output Low Voltage (Port 0, ALE, PSEN#) ^{4,5}	V _{DD} = 2.7 V I _{OL} = 200 μA ¹		0.3	V
		I _{OL} = 3.2 mA ¹		0.45	V
V _{OH}	Output High Voltage (Ports 1, 2, 3, ALE, PSEN#) ²	V _{DD} = 2.7 V I _{OH} = -10 μA	V _{DD} - 0.3		V
		I _{OH} = -30 μA	V _{DD} - 0.7		V
		I _{OH} = -60 μA	V _{DD} - 1.5		V
V _{OH1}	Output High Voltage (Port 0 in External Bus Mode) ²	V _{DD} = 2.7 V I _{OH} = -200 μA	V _{DD} - 0.3		V
		I _{OH} = -3.2 mA	V _{DD} - 0.7		V
I _{IL}	Logical 0 Input Current (Ports 1, 2, 3)	V _{IN} = 0.4V	-1	-75	μA
I _{TL}	Logical 1-to-0 Transition Current (Ports 1, 2, 3) ³	V _{IN} = 2V		-650	μA
I _{LI}	Input Leakage Current (Port 0)	0.45 < V _{IN} < V _{DD} -0.3		±10	μA
R _{RST}	RST Pulldown Resistor		40	225	kΩ
C _{IO}	Pin Capacitance ⁶	@ 1 MHz, 25°C		15	pF
I _{DD}	Power Supply Current ⁷ In-Application Mode Active Mode Idle Mode Standby (Stop Clock) Mode Power Down Mode	V _{DD} = 3 V		70	mA
					22
		T _{amb} = 0°C to +70°C		6.5	mA
				70	μA
		T _{amb} = -40°C to +85°C		88	μA
			V _{DD} = 2V		
	T _{amb} = 0°C to +70°C		40	μA	
	T _{amb} = -40°C to +85°C		50	μA	

325 PGM T12B.5



NOTES:

1. Capacitive loading on Ports 0 & 2 may cause spurious noise to be superimposed on the V_{OLs} of ALE and Ports 1 & 3. The noise due to external bus capacitance discharging into the Port 0 & 2 pins when the pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100pF), the noise pulse on the ALE pin may exceed 0.8V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input.
2. Capacitive loading on Ports 0 & 2 may cause the V_{OH} on ALE and PSEN# to momentarily fall below the $V_{DD} - 0.7$ specification when the address bits are stabilizing.
3. Pins of Ports 1, 2 & 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{in} is approximately 2V.
4. Load capacitance for Port 0, ALE & PSEN# = 100pF, load capacitance for all other outputs = 80pF.
5. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:

Maximum I_{OL} per port pin:	15mA
Maximum I_{OL} per 8-bit port:	26mA
Maximum I_{OL} total for all outputs:	71mA

If I_{OL} exceeds the test condition, V_{OH} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

6. Pin capacitance is characterized but not tested. EA# is 25pF.
7. See Figures 24, 25, 26 and 27 for test conditions. Minimum V_{DD} for Power Down is 2 V.

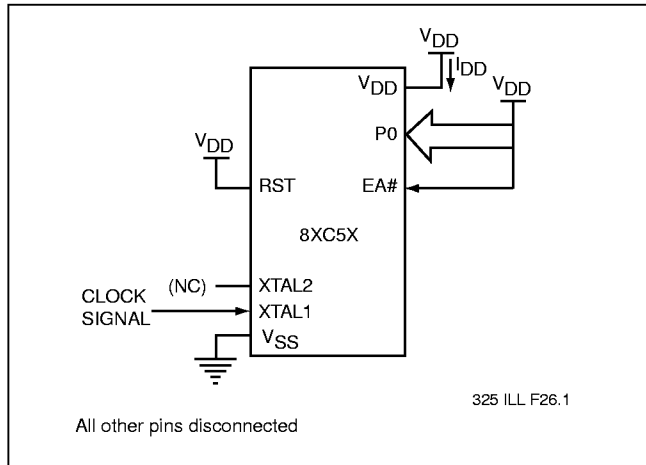


FIGURE 24: I_{DD} TEST CONDITION, ACTIVE MODE

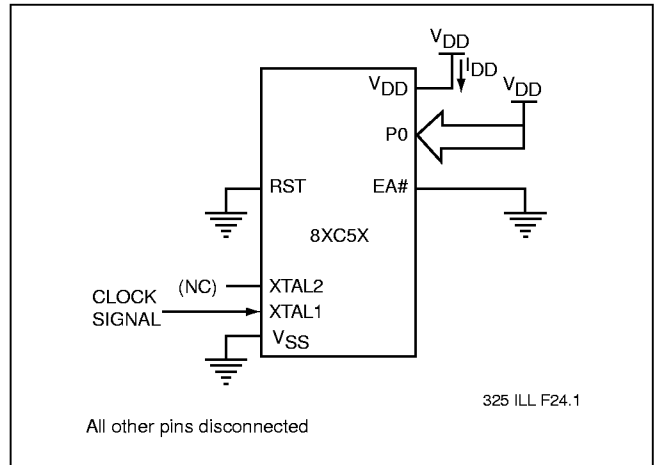


FIGURE 25: I_{DD} TEST CONDITION, IDLE MODE

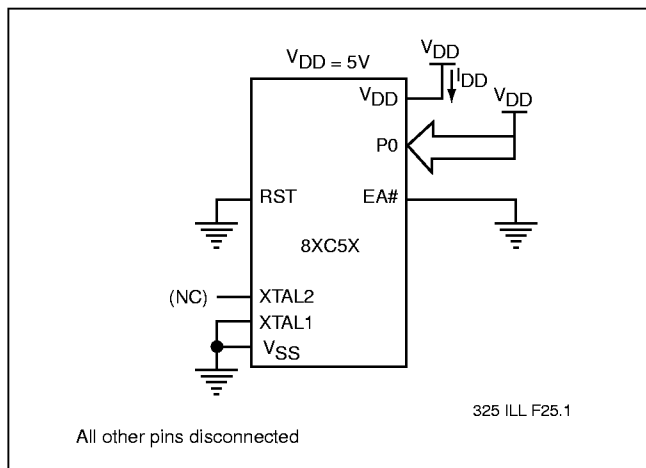


FIGURE 26: I_{DD} TEST CONDITION, POWER DOWN MODE

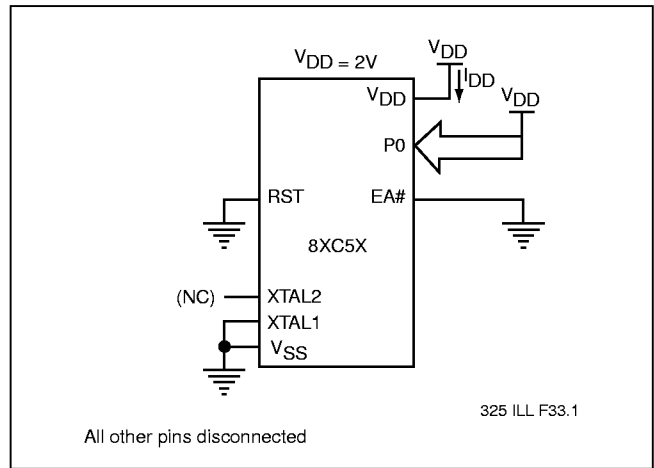


FIGURE 27: I_{DD} TEST CONDITION, STANDBY (STOP CLOCK) MODE



FlashFlex51 MCU

SST89C54 / SST89C58 / SST89C59

Advance Information

AC ELECTRICAL CHARACTERISTICS

AC Characteristics: (Over Operating Conditions; Load Capacitance for Port 0, ALE, and PSEN# = 100 pF; Load Capacitance for All Other Outputs = 80 pF)

TABLE 14: AC ELECTRICAL CHARACTERISTICS

T_{AMB} = 0° C TO +70° C OR -40° C TO +85° C, V_{DD} = 3V ±10% @ 12 MHz, 5V ±10% @ 33 MHz, V_{SS} = 0

Symbol	Parameter	Oscillator						Units
		12 MHz		33 MHz		Variable		
		Min	Max	Min	Max	Min.	Max.	
1/T _{CLCL}	Oscillator Frequency					0	33	MHz
T _{LHLL}	ALE Pulse Width	127		20		2T _{CLCL} - 40		ns
T _{AVLL}	Address Valid to ALE Low	43		5		T _{CLCL} - 40 T _{CLCL} - 25		ns ns
T _{LLAX}	Address Hold After ALE Low	53		5		T _{CLCL} - 30 T _{CLCL} - 25		ns ns
T _{LLIV}	ALE Low to Valid Instr In		234		56		4T _{CLCL} - 100 4T _{CLCL} - 65	ns ns
T _{LLPL}	ALE Low to PSEN# Low	53		5		T _{CLCL} - 30 T _{CLCL} - 25		ns ns
T _{PLPH}	PSEN# Pulse Width	205		46		3T _{CLCL} - 45		ns
T _{PLIV}	PSEN# Low to Valid Instr In		145		35		3T _{CLCL} - 105 3T _{CLCL} - 55	ns ns
T _{PIX}	Input Instr Hold After PSEN#					0		ns
T _{PIXZ}	Input Instr Float After PSEN#		59		5		T _{CLCL} - 25 T _{CLCL} - 25	ns ns
T _{AVIV}	Address to Valid Instr In		312		71		5T _{CLCL} - 105 5T _{CLCL} - 80	ns ns
T _{PLAZ}	PSEN# Low to Address Float		10		10		10	ns
T _{RLRH}	RD# Pulse Width	400		82		6T _{CLCL} - 100		ns
T _{WLWH}	Write Pulse Width (WE#)	400		82		6T _{CLCL} - 100		ns
T _{RLDV}	RD# Low to Valid Data In		252		61		5T _{CLCL} - 165 5T _{CLCL} - 90	ns ns
T _{RHDX}	Data Hold After RD#	0		0		0		ns
T _{RHDZ}	Data Float After RD#		107		35		2T _{CLCL} - 60 2T _{CLCL} - 25	ns ns
T _{LLDV}	ALE Low to Valid Data In		517		150		8T _{CLCL} - 150 8T _{CLCL} - 90	ns ns
T _{AVDV}	Address to Valid Data In		585		180		9T _{CLCL} - 165 9T _{CLCL} - 90	ns ns
T _{LLWL}	ALE Low to RD# or WR# Low	200	300	40	140	3T _{CLCL} - 50	3T _{CLCL} + 50	ns
T _{AVWL}	Address to RD# or WR# Low	203		46		4T _{CLCL} - 130 4T _{CLCL} - 75		ns ns
T _{QVWX}	Data Valid to WR# Transition	33		0		T _{CLCL} - 50 T _{CLCL} - 30		ns ns
T _{WHQX}	Data Hold After WR#	33		3		T _{CLCL} - 50 T _{CLCL} - 27		ns ns
T _{QVWH}	Data Valid to WR# High	433		140		7T _{CLCL} - 150 7T _{CLCL} - 70		ns ns
T _{RLAZ}	RD# Low to Address Float		0		0		0	ns
T _{WHLH}	RD# to WR# High to ALE High	43	123	5	55	T _{CLCL} - 40 T _{CLCL} - 25	T _{CLCL} + 40 T _{CLCL} + 25	ns ns
T _{VR} ¹	V _{DD} to Reset						10	ns

Note: 1. Refer to Figure 15 for minimum timing requirements for Power-On Reset.

325 PGM T13.4



AC CHARACTERISTICS

Explanation of Symbols

Each timing symbol has 5 characters. The first character is always a 'T' (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

- A: Address
- C: Clock
- D Input data
- H: Logic level HIGH
- I: Instruction (program memory contents).
- L: Logic level LOW or ALE

- P: PSEN#
- Q: Output data
- R: RD# signal
- T: Time
- V: Valid
- W: WR# signal
- X: No longer a valid logic level
- Z: High Impedance (Float)

For example:

T_{AVLL}=Time from Address Valid to ALE Low
T_{LLPL}=Time from ALE Low to PSEN# Low

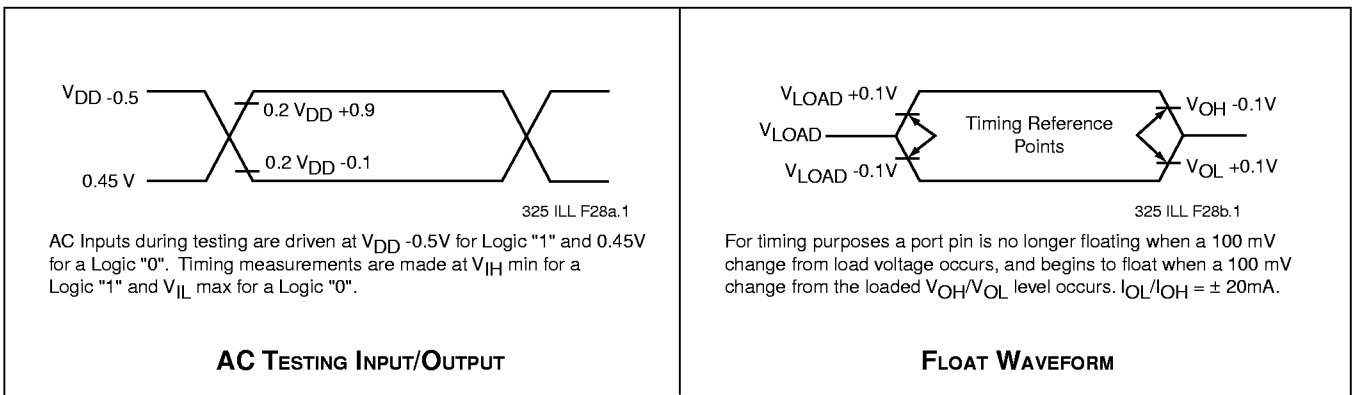
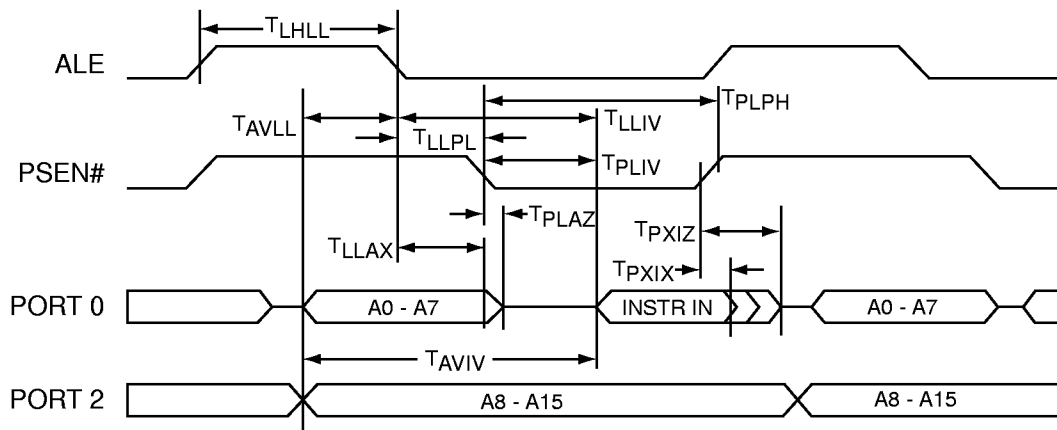


FIGURE 28: AC TESTING INPUT/OUTPUT, FLOAT WAVEFORM



325 ILL F13.6

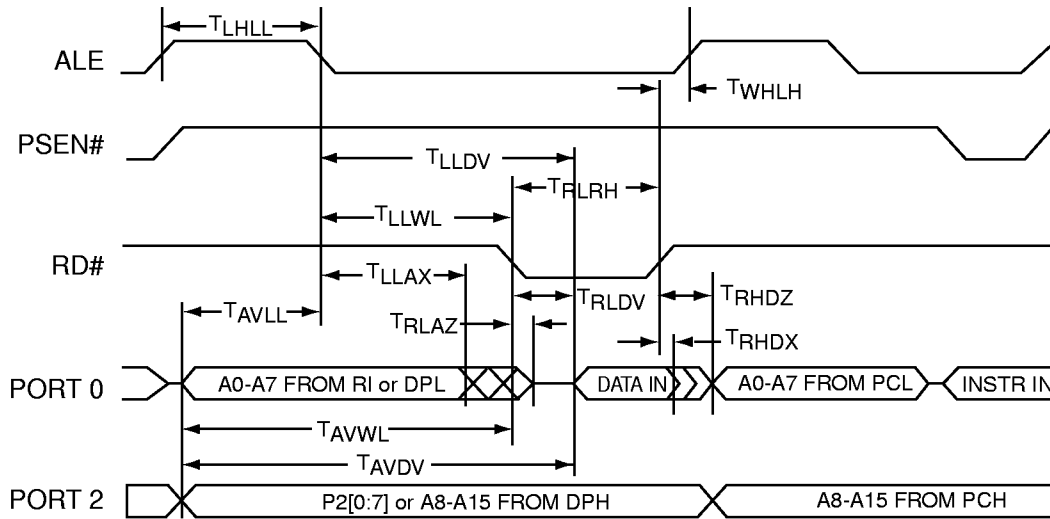
FIGURE 29: EXTERNAL PROGRAM MEMORY READ CYCLE



FlashFlex51 MCU

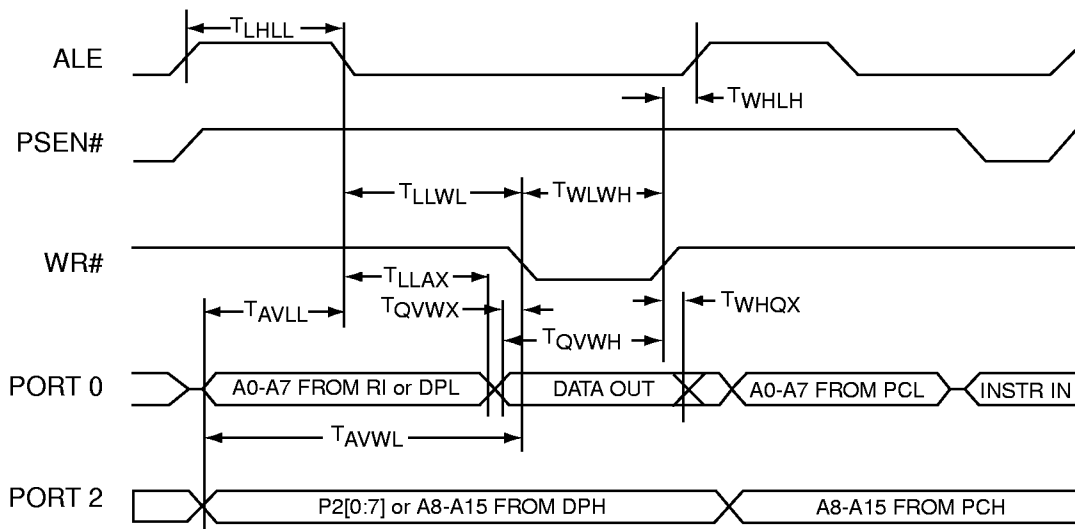
SST89C54 / SST89C58 / SST89C59

Advance Information



325 ILL F14.5

FIGURE 30: EXTERNAL DATA MEMORY READ CYCLE



325 ILL F15.5

FIGURE 31: EXTERNAL DATA MEMORY WRITE CYCLE

TABLE 15: EXTERNAL CLOCK DRIVE

Symbol	Parameter	Oscillator						Units
		12 MHz		33 MHz		Variable		
		Min	Max	Min	Max	Min.	Max.	
1/T _{CLCL}	Oscillator Frequency					0	33	MHz
T _{CHCX}	High Time					0.35T _{CLCL}	0.65T _{CLCL}	ns
T _{CLCX}	Low Time					0.35T _{CLCL}	0.65T _{CLCL}	ns
T _{CLCH}	Rise Time				5		20	ns
T _{CHCL}	Fall Time				5		20	ns

325 PGM T14.3

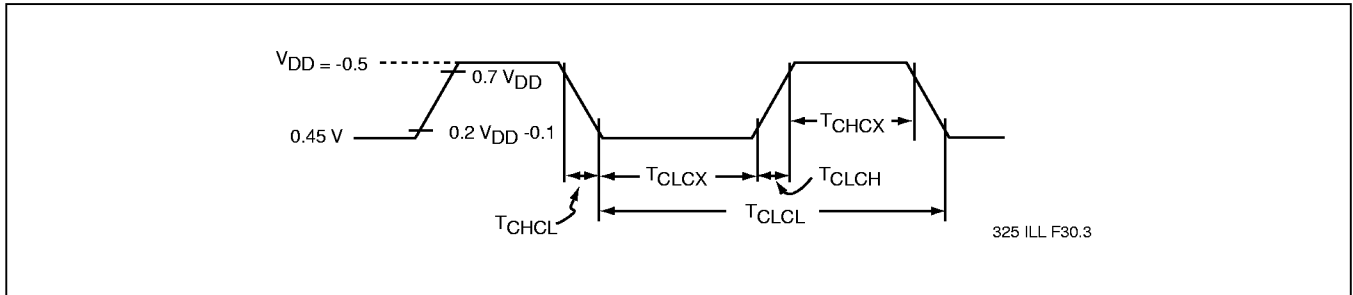
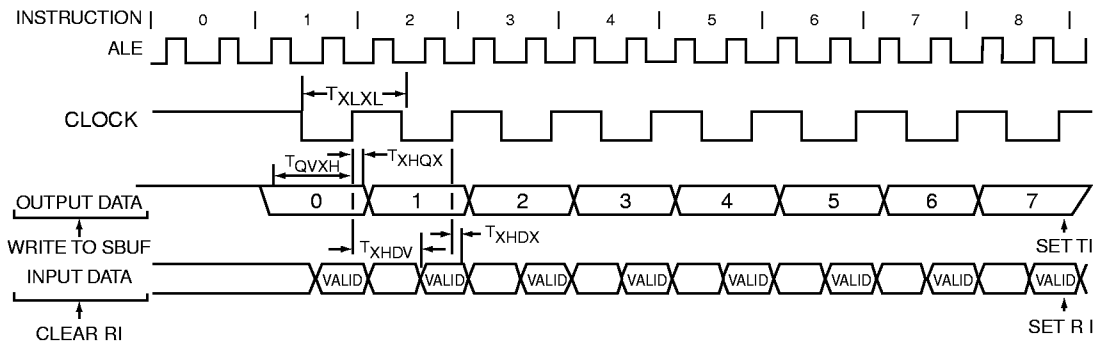


FIGURE 32: EXTERNAL CLOCK DRIVE WAVEFORM

TABLE 16: SERIAL PORT TIMING

Symbol	Parameter	Oscillator						Units
		12 MHz		33 MHz		Variable		
		Min	Max	Min	Max	Min.	Max.	
T _{XLXL}	Serial Port Clock Cycle Time	0		0.36		12T _{CLCL}		ms
T _{QVXH}	Output Data Setup to Clock Rising Edge	700		167		10T _{CLCL} - 133		ns
T _{XHQX}	Output Data Hold After Clock Rising Edge	50		10		2T _{CLCL} - 117 2T _{CLCL} - 50		ns ns
T _{XHDX}	Input Data Hold After Clock Rising Edge	0		0		0		ns
T _{XHDV}	Clock Rising Edge to Input Data Valid		700		167		10T _{CLCL} - 133	ns

325 PGM T15.2



325 ILL F29.2

FIGURE 33: SHIFT REGISTER MODE TIMING WAVEFORMS



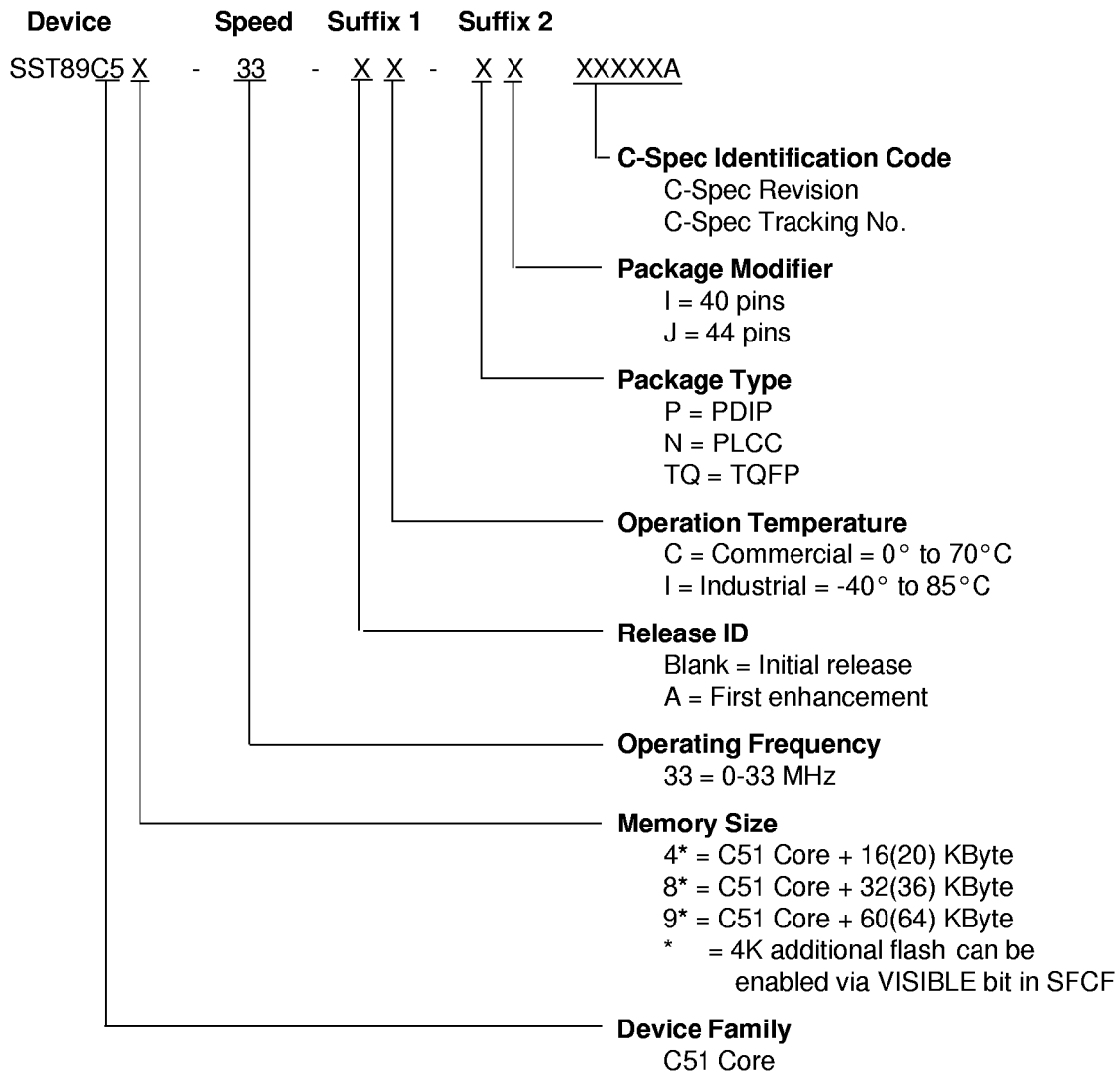
FlashFlex51 MCU

SST89C54 / SST89C58 / SST89C59

Advance Information

PRODUCT ORDERING INFORMATION

Product Identification Descriptor





Part Number Valid Combinations

SST89C54 Valid combinations

<i>Part Number</i>	<i>Package</i>	<i>Pins</i>	<i>V_{DD}</i>	<i>Speed</i>	<i>Temperature</i>
SST89C54-33-C-PI	PDIP	40	2.7-5.5	0-33MHz	Commercial
SST89C54-33-C-NJ	PLCC	44	2.7-5.5	0-33MHz	Commercial
SST89C54-33-C-TQJ	TQFP	44	2.7-5.5	0-33MHz	Commercial
SST89C54-33-I-PI	PDIP	40	2.7-5.5	0-33MHz	Industrial
SST89C54-33-I-NJ	PLCC	44	2.7-5.5	0-33MHz	Industrial
SST89C54-33-I-TQJ	TQFP	44	2.7-5.5	0-33MHz	Industrial

SST89C58 Valid combinations

<i>Part Number</i>	<i>Package</i>	<i>Pins</i>	<i>V_{DD}</i>	<i>Speed</i>	<i>Temperature</i>
SST89C58-33-C-PI	PDIP	40	2.7-5.5	0-33MHz	Commercial
SST89C58-33-C-NJ	PLCC	44	2.7-5.5	0-33MHz	Commercial
SST89C58-33-C-TQJ	TQFP	44	2.7-5.5	0-33MHz	Commercial
SST89C58-33-I-PI	PDIP	40	2.7-5.5	0-33MHz	Industrial
SST89C58-33-I-NJ	PLCC	44	2.7-5.5	0-33MHz	Industrial
SST89C58-33-I-TQJ	TQFP	44	2.7-5.5	0-33MHz	Industrial

SST89C59 Valid combinations

<i>Part Number</i>	<i>Package</i>	<i>Pins</i>	<i>V_{DD}</i>	<i>Speed</i>	<i>Temperature</i>
SST89C59-33-C-PI	PDIP	40	2.7-5.5	0-33MHz	Commercial
SST89C59-33-C-NJ	PLCC	44	2.7-5.5	0-33MHz	Commercial
SST89C59-33-C-TQJ	TQFP	44	2.7-5.5	0-33MHz	Commercial
SST89C59-33-I-PI	PDIP	40	2.7-5.5	0-33MHz	Industrial
SST89C59-33-I-NJ	PLCC	44	2.7-5.5	0-33MHz	Industrial
SST89C59-33-I-TQJ	TQFP	44	2.7-5.5	0-33MHz	Industrial

Example: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability and to determine availability of new combinations.



FlashFlex51 MCU

SST89C54 / SST89C58 / SST89C59

Advance Information

Part Number Cross-Reference Guide

Intel		SST		package
i87C54	16K EPROM & 256B RAM	SST89C54	4K Flash, 16K Flash & 256B RAM	D L Q
i87C58	32K EPROM & 256B RAM	SST89C58	4K Flash, 32K Flash & 256B RAM	D L Q
i87L54	16K ROM (OTP) & 256B RAM	SST89C54	4K Flash, 16K Flash & 256B RAM	L Q
i87L58	32K ROM (OTP) & 256B RAM	SST89C58	4K Flash, 32K Flash & 256B RAM	L Q
i87C51FB	16K EPROM & 256B RAM	SST89C54*	4K Flash, 16K Flash & 256B RAM	D L Q
i87C51FC	32K EPROM & 256B RAM	SST89C58*	4K Flash, 32K Flash & 256B RAM	D L Q
Atmel				
AT89C52	8K Flash & 256B RAM	SST		package
AT89LV52	8K Flash & 256B RAM	SST89C54	4K Flash, 16K Flash & 256B RAM	D L Q
AT89S53	12K Flash & 256B RAM	SST89C54	4K Flash, 16K Flash & 256B RAM	D L Q
AT89LS53	12K Flash & 256B RAM	SST89C54*	4K Flash, 16K Flash & 256B RAM	D L Q
AT89C55	20K Flash & 256B RAM	SST89C58*	4K Flash, 32K Flash & 256B RAM	D L Q
AT89LV55	20K Flash & 256B RAM	SST89C58*	4K Flash, 32K Flash & 256B RAM	D L Q
Temic				
80C51	4K ROM & 256B RAM	SST		package
80C52	8K ROM & 256B RAM	SST89C54*	4K Flash, 16K Flash & 256B RAM	D L Q
83C154	16K ROM & 256B RAM	SST89C54	4K Flash, 16K Flash & 256B RAM	D L Q
83C154D	32K ROM & 256B RAM	SST89C54	4K Flash, 16K Flash & 256B RAM	D L Q
87C51	4K EPROM & 256B RAM	SST89C58	4K Flash, 32K Flash & 256B RAM	D L Q
87C52	8K EPROM & 256B RAM	SST89C54*	4K Flash, 16K Flash & 256B RAM	D L Q
Philips				
P80C54	16K ROM & 256B RAM	SST		package
P80C58	32K ROM & 256B RAM	SST89C54	4K Flash, 16K Flash & 256B RAM	D L Q
P87C54	16K EPROM & 256B RAM	SST89C58	4K Flash, 32K Flash & 256B RAM	D L Q
P87C58	32K EPROM & 256B RAM	SST89C54	4K Flash, 16K Flash & 256B RAM	D L Q
P87C524	16K EPROM & 512B RAM	SST89C58	4K Flash, 32K Flash & 256B RAM	D L Q
P87C528	32K EPROM & 512B RAM	SST89C54*	4K Flash, 16K Flash & 256B RAM	D L Q
P83C524	16K ROM & 512B RAM	SST89C58*	4K Flash, 32K Flash & 256B RAM	D L
P83C528	32K MROM & 512B RAM	SST89C54*	4K Flash, 16K Flash & 256B RAM	D L Q
P89CE558	32K Flash & 1K RAM	SST89C58*	4K Flash, 32K Flash & 256B RAM	D L Q
Winbond				
W78C54	16K MROM & 256B RAM	SST		package
W78C58	32K MROM & 256B RAM	SST89C54	4K Flash, 16K Flash & 256B RAM	D L Q
W78E54	16K EEPROM & 256B RAM	SST89C58	4K Flash, 32K Flash & 256B RAM	D L Q
W78E58	32K EEPROM & 256B RAM	SST89C54	4K Flash, 16K Flash & 256B RAM	D L Q
ISSI				
IS80C52	8K ROM & 256B RAM	SST		package
		SST89C54	4K Flash, 16K Flash & 256B RAM	D L Q
Dallas				
DS83C520	16K MROM & 256B RAM	SST		package
DS87C520	16K EPROM (OTP) &	SST89C54*	4K Flash, 16K Flash & 256B RAM	D L Q
256B RAM		SST89C54*	4K Flash, 16K Flash & 256B RAM	D L Q
Siemens				
C501-1R	8K ROM & 256B RAM	SST		package
C501-1E	8K ROM (OTP) & 256B RAM	SST89C54	4K Flash, 16K Flash & 256B RAM	D L
C513A-H	12K EPROM & 512B RAM	SST89C54	4K Flash, 16K Flash & 256B RAM	D L
C503-1R	8K ROM & 256B RAM	SST89C54*	4K Flash, 16K Flash & 256B RAM	L
C504-2R	16K ROM & 512B RAM	SST89C54*	4K Flash, 16K Flash & 256B RAM	L
		SST89C54*	4K Flash, 16K Flash & 256B RAM	Q

D: PDIP
L: PLCC
Q: TQFP

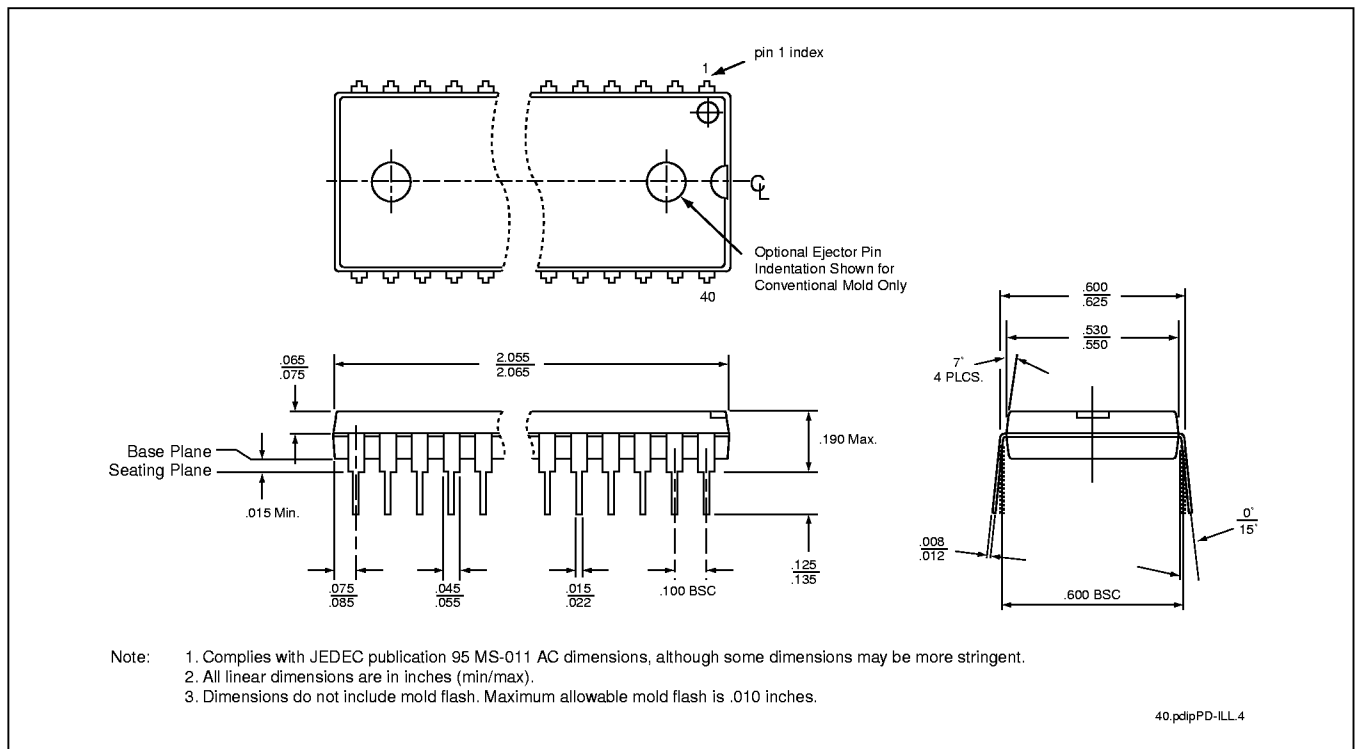
NOTE: The SST89C58 can be substituted for any SST89C54 listing above.

NOTE: The SST89C59 can be substituted for any SST89C54 or SST89C58 listing above.

* Indicates SST similar function and not direct replacement/socket compatible.

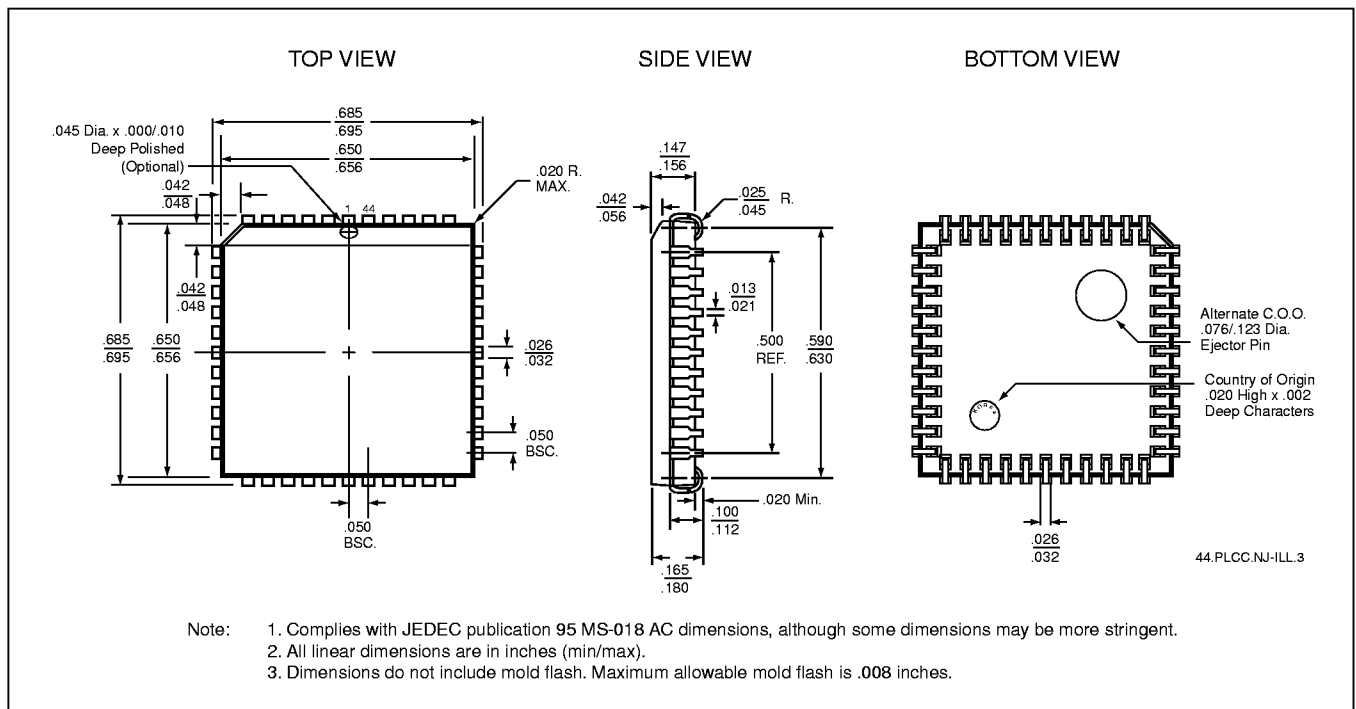


PACKAGING DIAGRAMS



40-LEAD PLASTIC DUAL-IN-LINE PACKAGE (PDIP)

SST PACKAGE CODE: PI



44-LEAD PLASTIC LEAD CHIP CARRIER (PLCC)

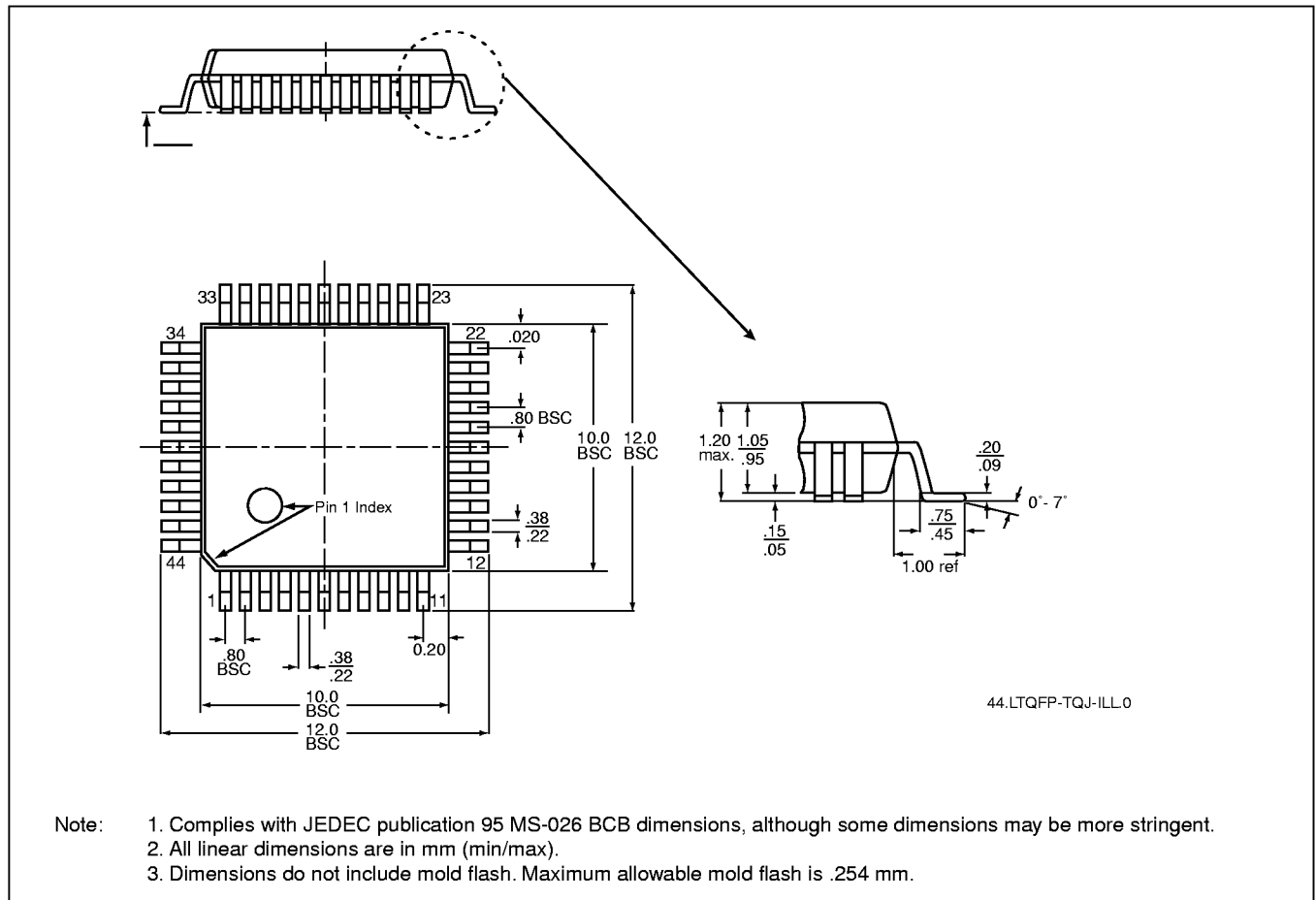
SST PACKAGE CODE: NJ



FlashFlex51 MCU

SST89C54 / SST89C58 / SST89C59

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44-LEAD THIN QUAD FLAT PACK (TQFP)
SST PACKAGE CODE: TQJ