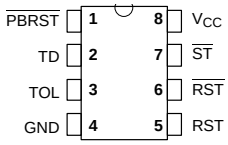
DALLAS SEMICONDUCTOR

DS1232LP/LPS
Low Power MicroMonitor Chip

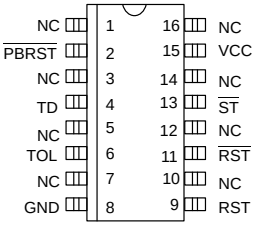
FEATURES

- Super low-power version of DS1232
- 50 μA quiescent current
- Halts and restarts an out–of–control microprocessor
- Automatically restarts microprocessor after power failure
- Monitors pushbutton for external override
- Accurate 5% or 10% microprocessor power supply monitoring
- 8–pin DIP, 8–pin SOIC or space saving μ–SOP package available
- Optional 16–pin SOIC package available
- Industrial temperature –40°C to +85°C available, designated N

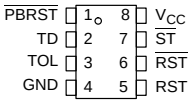
PIN ASSIGNMENT



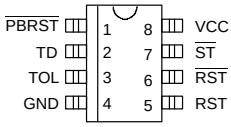
DS1232LP 8–Pin DIP
(300 Mil)
See Mech. Drawings Section



DS1232LPS 16–Pin SOIC
(300 Mil)
See Mech. Drawings Section



DS1232LPμ
(118 MIL μ–SOP)
See Mech. Drawings Section



DS1232LPS–2 8–Pin SOIC
(150 Mil)
See Mech. Drawings Section

PIN DESCRIPTION

$\overline{\text{PBRST}}$	–	Pushbutton Reset Input
TD	–	Time Delay Set
TOL	–	Selects 5% or 10% V_{CC} Detect
GND	–	Ground
RST	–	Reset Output (Active High)
$\overline{\text{RST}}$	–	Reset Output (Active Low, open drain)
$\overline{\text{ST}}$	–	Strobe Input
V_{CC}	–	+5 Volt Power

DESCRIPTION

The DS1232LP/LPS Low Power MicroMonitor Chip monitors three vital conditions for a microprocessor: power supply, software execution, and external override. First, a precision temperature–compensated reference and comparator circuit monitors the status of V_{CC}. When an out–of–tolerance condition occurs, an internal power fail signal is generated which forces reset to the active state. When V_{CC} returns to an in-tolerance condition, the reset signals are kept in the active state for a minimum of 250 ms to allow the power supply and processor to stabilize.

The second function the DS1232LP/LPS performs is pushbutton reset control. The DS1232LP/LPS debounces the pushbutton input and guarantees an active reset pulse width of 250 ms minimum. The third function is a watchdog timer. The DS1232LP/LPS has an internal timer that forces the reset signals to the active state if

the strobe input is not driven low prior to time–out. The watchdog timer function can be set to operate on time-out settings of approximately 150 ms, 600 ms, and 1.2 seconds.

OPERATION – POWER MONITOR

The DS1232LP/LPS detects out–of–tolerance power supply conditions and warns a processor–based system of impending power failure. When V_{CC} falls below a preset level as defined by TOL, the V_{CC} comparator outputs the signals RST and $\overline{RST}$. When TOL is connected to ground, the RST and $\overline{RST}$ signals become active as V_{CC} falls below 4.75 volts. When TOL is connected to V_{CC}, the RST and $\overline{RST}$ signals become active as V_{CC} falls below 4.5 volts. The RST and $\overline{RST}$ are excellent control signals for a microprocessor, as processing is stopped at the last possible moments of valid V_{CC}. On power–up, RST and $\overline{RST}$ are kept active for a minimum of 250 ms to allow the power supply and processor to stabilize.

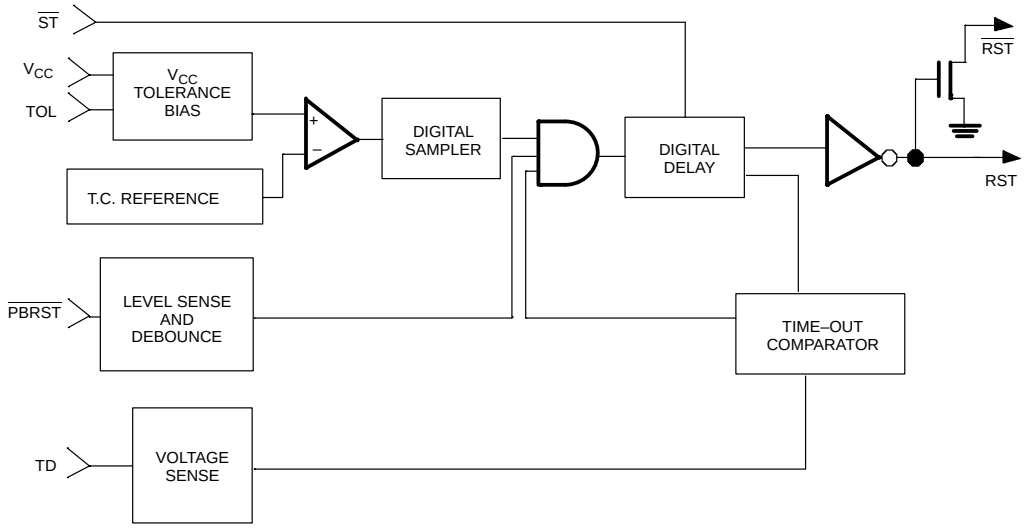
OPERATION – PUSHBUTTON RESET

The DS1232LP/LPS provides an input pin for direct connection to a pushbutton (Figure 1). The pushbutton reset input requires an active low signal. Internally, this input is debounced and timed such that RST and $\overline{RST}$ signals of at least 250 ms minimum are generated. The 250 ms delay starts as the pushbutton reset input is released from low level.

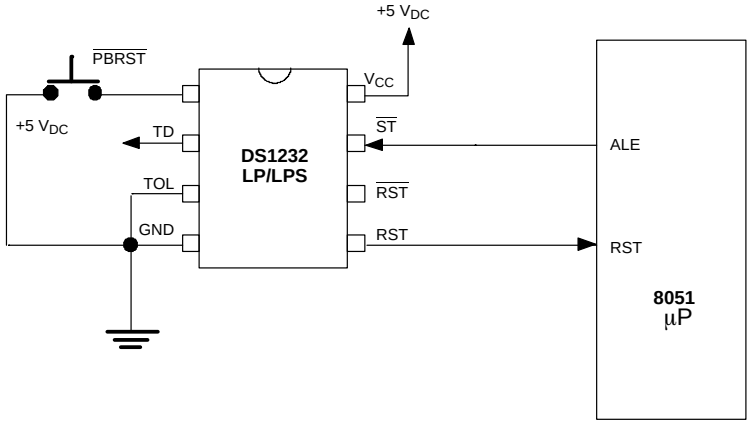
OPERATION – WATCHDOG TIMER

The watchdog timer function forces RST and $\overline{RST}$ signals to the active state when the $\overline{ST}$ input is not stimulated for a predetermined time period. The time period is set by the TD input to be typically 150 ms with TD connected to ground, 600 ms with TD left unconnected, and 1.2 seconds with TD connected to V_{CC}. The watchdog timer starts timing out from the set time period as soon as RST and $\overline{RST}$ are inactive. If a high–to–low transition occurs on the $\overline{ST}$ input pin prior to time–out, the watchdog timer is reset and begins to time–out again. If the watchdog timer is allowed to time-out, then the RST and $\overline{RST}$ signals are driven to the active state for 250 ms minimum. The $\overline{ST}$ input can be derived from microprocessor address signals, data signals, and/or control signals. When the microprocessor is functioning normally, these signals would, as a matter of routine, cause the watchdog to be reset prior to time–out. To guarantee that the watchdog timer does not time–out, a high–to–low transition must occur at or less than the minimum shown in Table 1. A typical circuit example is shown in Figure 2.

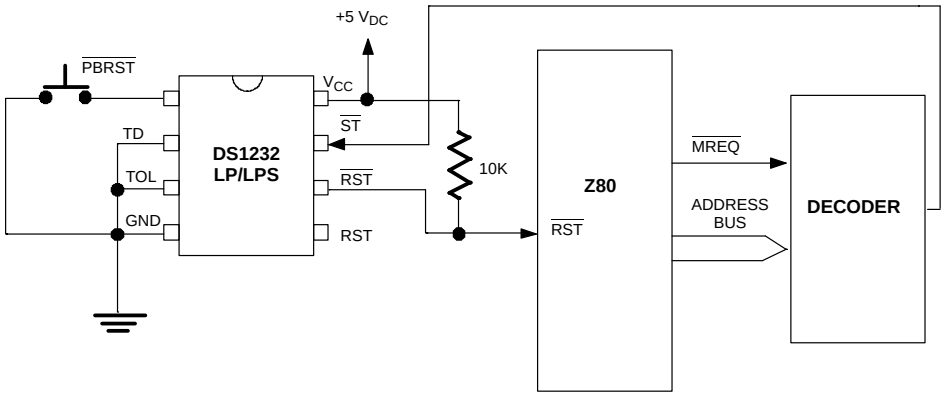
MICROMONITOR BLOCK DIAGRAM



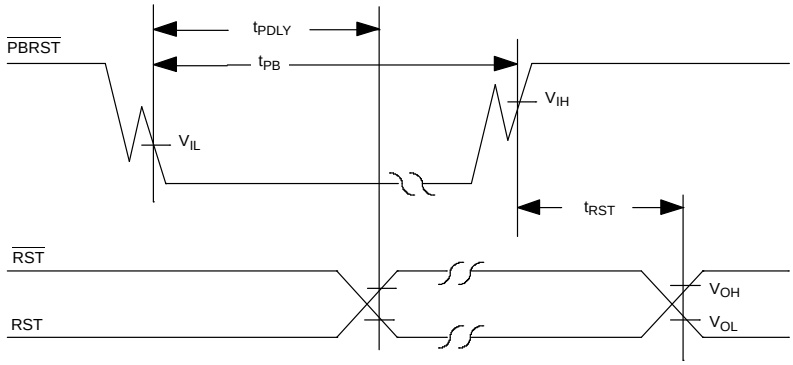
PUSHBUTTON RESET Figure 1



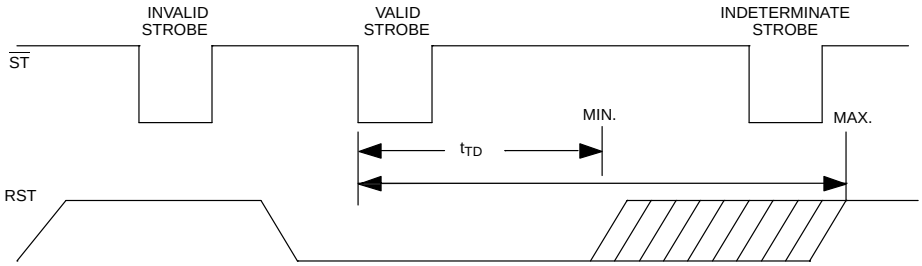
WATCHDOG TIMER Figure 2



TIMING DIAGRAM: PUSHBUTTON RESET Figure 3



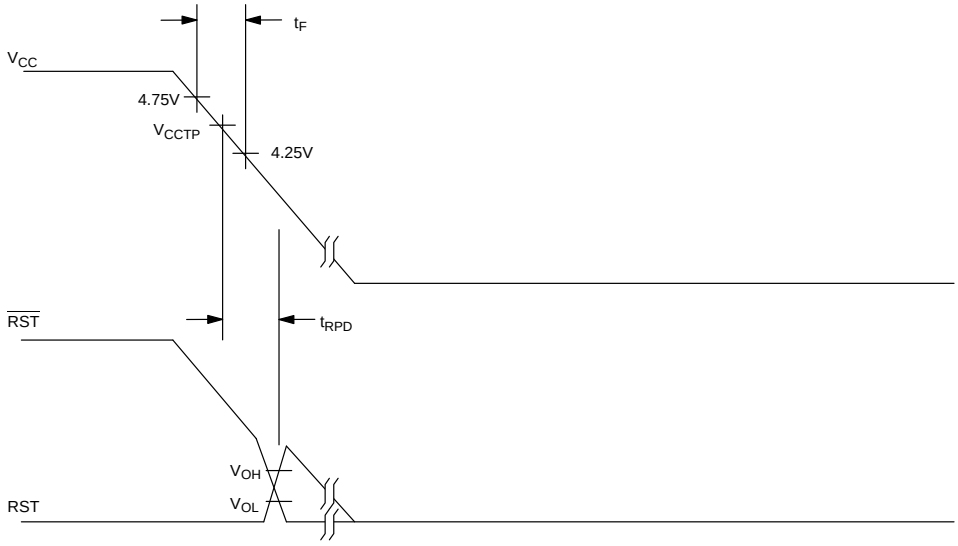
TIMING DIAGRAM: STROBE INPUT Figure 4



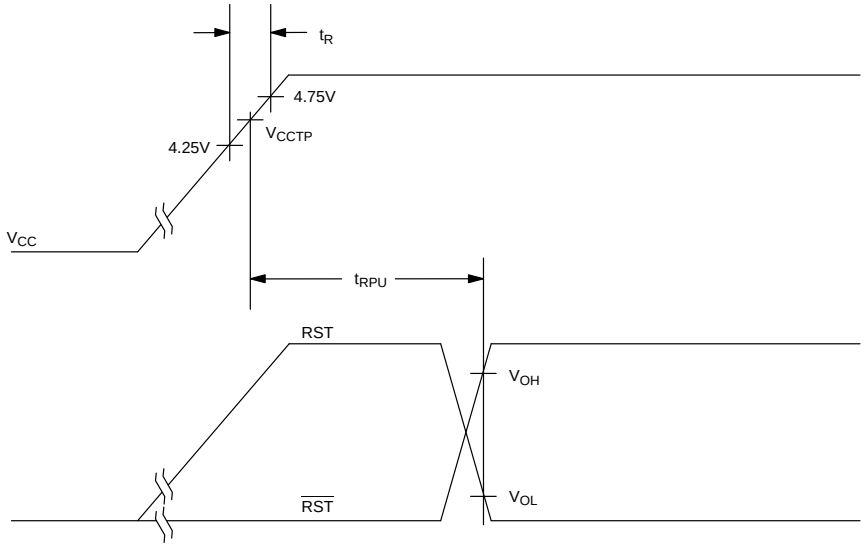
WATCHDOG TIME–OUTS Table 1

TD	TIME–OUT		
	MIN	**TYP**	**MAX**
GND	62.5 ms	150 ms	250 ms
Float	250 ms	600 ms	1000 ms
V_{CC}	500 ms	1200 ms	2000 ms

TIMING DIAGRAM: POWER DOWN Figure 5



TIMING DIAGRAM: POWER UP Figure 6



ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Pin Relative to Ground	–0.5V to +7.0V
Voltage on I/O Relative to Ground	–0.5V to V_{CC} + 0.5V
Operating Temperature	0°C to 70°C
Operating Temperature (Industrial Version)	–40°C to +85°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
$\overline{ST}$ and $\overline{PBRST}$ Input High Level	V_{IH}	2.0		V_{CC}+0.3	V	1
$\overline{ST}$ and $\overline{PBRST}$ Input Low Level	V_{IL}	–0.3		+0.8	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{IL}	–1.0		+1.0	µA	3
Output Current @ 2.4V	I_{OH}	–8	–10		mA	5
Output Current @ 0.4V	I_{OL}	10			mA	
Low Level @ RST	V_{OL}			0.4	V	1
Output Voltage @ –500 uA	V_{OH}	V_{CC} –0.5V	V_{CC} –0.1V		V	1, 7
Operating Current (CMOS)	I_{CC1}			50	µA	2
Operating Current (TTL)	I_{CC2}		200	500	µA	8
V_{CC} Trip Point (TOL = GND)	V_{CCTP}	4.50	4.62	4.74	V	1
V_{CC} Trip Point (TOL = V_{CC})	V_{CCTP}	4.25	4.37	4.49	V	1

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

AC ELECTRICAL CHARACTERISTICS (0°C to 70°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{PBRST}$ = V_{IL}	t_{PB}	20			ms	
RESET Active Time	t_{RST}	250	610	1000	ms	
$\overline{ST}$ Pulse Width	t_{ST}	20			ns	6, 9
V_{CC} Fail Detect to RST and $\overline{RST}$	t_{RPD}		50	175	µs	
V_{CC} Slew Rate 4.75V to 4.25V	t_F	300			µs	
V_{CC} Detect to RST and $\overline{RST}$ Inactive	t_{RPU}	250	610	1000	ms	4
V_{CC} Slew Rate 4.25V to 4.75V	t_R	0			ns	
$\overline{PBRST}$ Stable Low to $\overline{RST}$ and RST	t_{PDLY}			20	ms	

NOTES:

1. All voltages referenced to ground.
2. Measured with outputs open and $\overline{ST}$ and $\overline{PBRST}$ within 0.5V of supply rails.
3. $\overline{PBRST}$ is internally pulled up to V_{CC} with an internal impedance of 40K typical.
4. t_R = 5 µs.
5. $\overline{RST}$ is an open drain output.
6. Must not exceed t_{TD} minimum. See Table 1.
7. RST remains within 0.5V of V_{CC} on power–down until V_{CC} drops below 2.0V. $\overline{RST}$ remains within 0.5V of GND on power–down until V_{CC} drops below 2.0V.
8. Measured with outputs open and $\overline{ST}$ and $\overline{PBRST}$ at TTL levels.
9. Watchdog can not be disabled. It must be strobed to avoid resets.

MARKING INFORMATION:

8–pin DIP – “DS1232L”
16–pin SOIC – “DS1232L”
8–pin SOIC – “DS1232L”
8–pin µ–SOP – “1232”