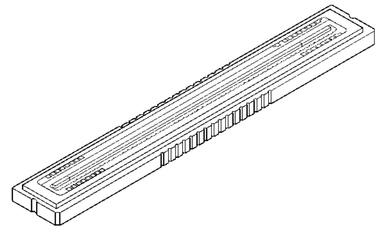
TOSHIBA CCD Linear Image Sensor Silicon Monolithic
CCD (charge coupled device)

TCD2964BFG

The TCD2964BFG is a high sensitive and low dark current 21360 elements × 6 line CCD color image sensor. The sensor is designed for scanner.

The device contains a row of 21360 elements × 6 line staggered photodiodes which provide a 192 lines/mm (4800DPI) across a A4 size paper. The device is operated by 5 V pulse and 12 V power supply.



WQFN32-C-R300-1.27C

Weight: 3.2 g (typ.)

Features

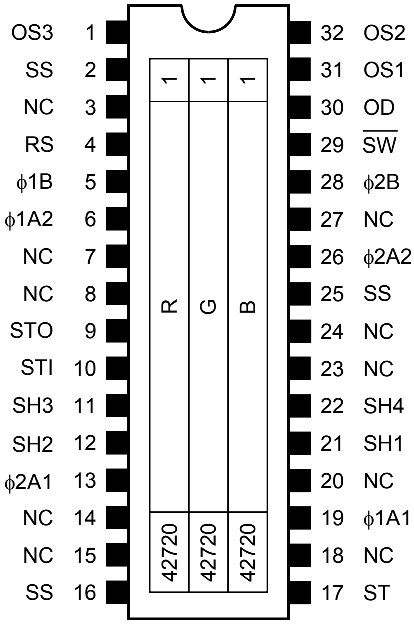
- Number of Image Sensing Elements: 21360 elements × 6 line
- Image Sensing Element Size: 2 μm by 4 μm on 2 μm centers
- Photo Sensing Region: High sensitive and low dark current PN photodiode
- Distance between Photodiode Array: 64 μm (32 lines), Red line-Green line, Green line-Blue line
  6 μm (3 lines), Odd line-Even-line
- Clock: 2 phase (5 V)
- Power Supply: 12 V Power Supply Voltage
- Package: 32pin CLCC package
- Color Filter: Red, Green, Blue
- Overflow drain for antiblooming

ABSOLUTE MAXIMUM RATINGS (Note 1)

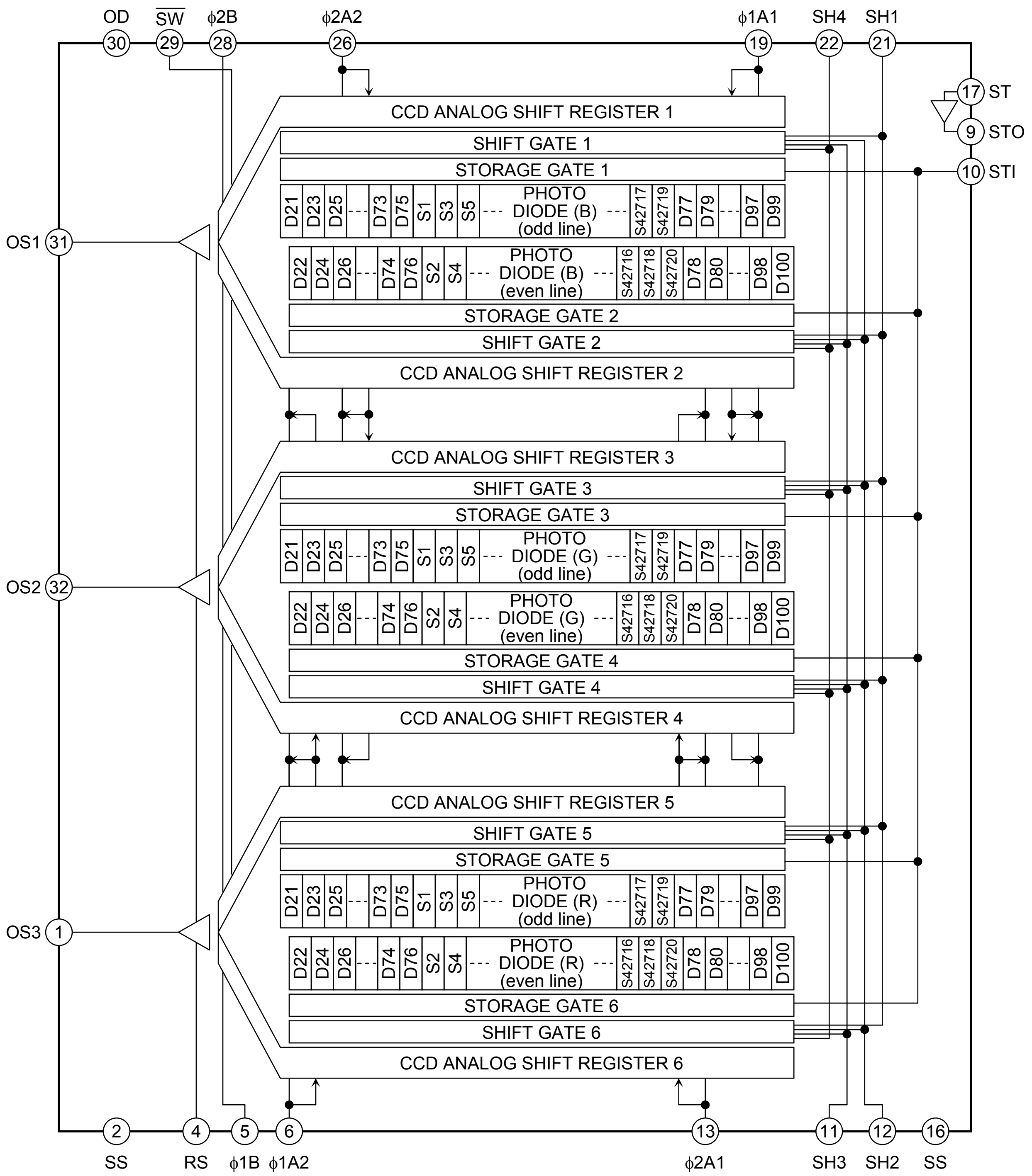
Characteristics	Symbol	Rating	Unit
Clock pulse voltage	V_{ϕ}	−0.3~8.0	V
Storage pulse voltage	V_{ST}		V
Shift pulse voltage	V_{SH}		V
Reset pulse voltage	V_{RS}		V
Switch pulse voltage	$V_{\overline{SW}}$		V
Storage pulse input voltage	V_{STI}	−3~15	V
Power supply voltage	V_{OD}	−0.3~15	V
Operating temperature	T_{opr}	0~60	°C
Storage temperature	T_{stg}	−25~85	°C

Note 1: All voltage are with respect to SS terminals (ground).
None of the ABSOLUTE MAXIMUM RATINGS must be exceeded, even instantaneously.
If any one of the ABSOLUTE MAXIMUM RATINGS is exceeded, the electrical characteristics, reliability and life time of the device cannot be guaranteed.
If the ABSOLUTE MAXIMUM RATINGS are exceeded, the device can be permanently damaged or degraded.
Create a system design in such a manner that any of the ABSOLUTE MAXIMUM RATINGS will not be exceeded under any circumstances.

Pin Connections (top view)



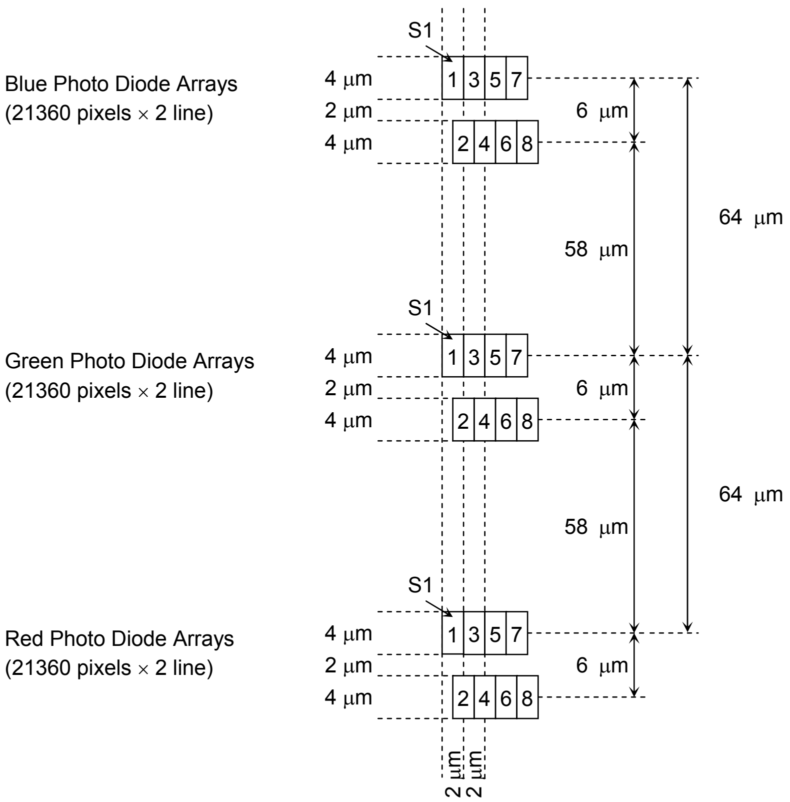
Circuit Diagram



Pin Names

Pin No.	Symbol	Name	Pin No.	Symbol	Name
1	OS3	Signal output 3 (red)	32	OS2	Signal output 2 (green)
2	SS	Ground	31	OS1	Signal output 1 (blue)
3	NC	Non connection	30	OD	Power
4	RS	Reset gate	29	$\overline{SW}$	Switch gate
5	$\phi 1B$	Final stage clock (phase 1)	28	$\phi 2B$	Final stage clock (phase 2)
6	$\phi 1A2$	Clock 2 (phase 1)	27	NC	Non connection
7	NC	Non connection	26	$\phi 2A2$	Clock 2 (phase 2)
8	NC	Non connection	25	SS	Ground
9	STO	Storage pulse output	24	NC	Non connection
10	STI	Storage pulse input	23	NC	Non connection
11	SH3	Shift gate 3	22	SH4	Shift gate 4
12	SH2	Shift gate 2	21	SH1	Shift gate 1
13	$\phi 2A1$	Clock 1 (phase 2)	20	NC	Non connection
14	NC	Non connection	19	$\phi 1A1$	Clock 1 (phase 1)
15	NC	Non connection	18	NC	Non connection
16	SS	Ground	17	ST	Storage gate

Arrangement of the 1st Effective Pixel (S1)



Optical/Electrical Characteristics

(Ta = 25°C, V_{OD} = 12 V, V_{ϕ} = V_{RS} = 5 V (pulse), V_{ST} = V_{SH} = 3.3 V (pulse), f_{ϕ} = 1 MHz, f_{RS} = 2 MHz, t_{INT} = 22 ms, LIGHT SOURCE = A LIGHT SOURCE + CM500S FILTER (t = 1 mm), LOAD RESISTANCE = 100 kΩ)

Characteristics		Symbol	Min	Typ.	Max	Unit	Note
Sensitivity	Red	$R_{(R)}$	0.9	1.3	1.7	V/lx・s	(Note 2)
	Green	$R_{(G)}$	1.0	1.5	2.0		
	Blue	$R_{(B)}$	0.4	0.7	1.0		
Photo response non uniformity		PRNU (1)	—	10	20	%	(Note 3)
		PRNU (3)	—	3	12	mV	(Note 4)
Register imbalance		RI	—	1	3	%	(Note 5)
Saturation output voltage		V_{SAT}	2.4	2.8	—	V	(Note 6)
Saturation exposure		SE	—	1.87	—	lx・s	(Note 7)
Dark signal voltage		V_{DRK}	—	0.6	2.7	mV	(Note 8)
Dark signal non uniformity		DSNU	—	6.6	9.2	mV	(Note 8)
DC power dissipation		P_D	—	360	470	mW	—
Total transfer efficiency		TTE	92	98	—	%	—
Output impedance		Z_O	—	0.2	0.5	kΩ	—
DC output voltage		V_{OS}	4.8	5.8	6.8	V	(Note 9)
Reset noise		V_{RSN}	—	0.4	1.0	V	(Note 9)
Random noise		NDσ	—	0.7	—	mV	(Note 10)

Note 2: Sensitivity is defined for each color of signal outputs average when the photosensitive surface is applied with the light of uniform illumination and uniform color temperature.

Note 3: PRNU (1) is defined for each color on a single chip by the expressions below when the photosensitive surface is applied with the light of uniform illumination and uniform color temperature.

$$\mathrm{PRNU\ (1)} = \frac{\Delta x}{\overline{x}} \times 100\ (\%)$$

Where $\overline{x}$ is average of total signal output and Δx is the maximum deviation from $\overline{x}$. The amount of incident light is shown below.

Red = 1/2·SE
Green = 1/2·SE
Blue = 1/4·SE

Note 4: PRNU (3) is defined as maximum voltage with next pixels, where measured at 5% of SE (typ.).

Note 5: Register imbalance is defined as follows.

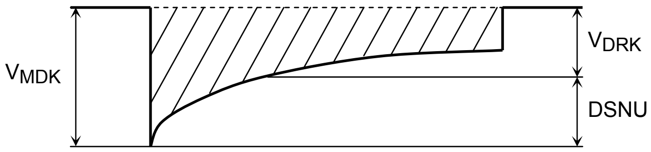
$$\mathrm{RI} = \frac{\sum_{n=1}^{42719} \left| xn - x(n+1) \right|}{42719 \times \overline{x}} \times 100\ (\%)$$

Note 6: V_{SAT} is defined as minimum saturation output of all effective pixels.

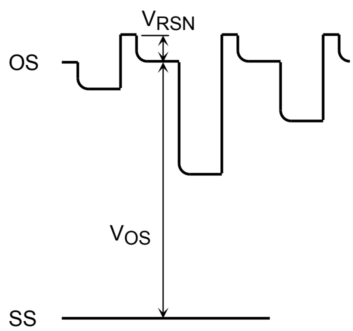
Note 7: Definition of SE

$$\mathrm{SE} = \frac{V_{SAT}}{R_G}\ (\mathrm{lx \cdot s})$$

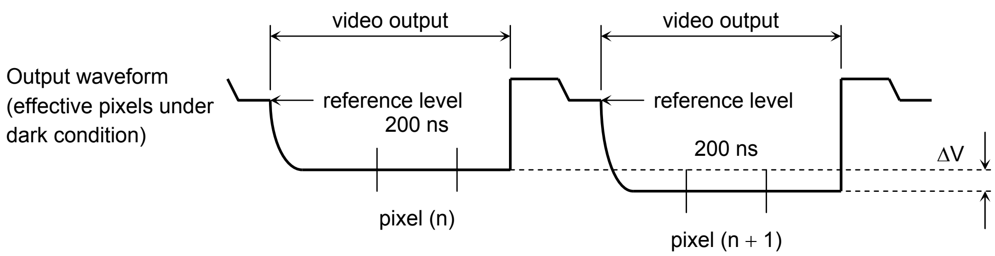
Note 8: V_{DRK} and DSNU are defined at t_{INT} = 14.55ms.
V_{DRK} is defined as average dark signal voltage of all effective pixels. DSNU is defined as different voltage between V_{DRK} and V_{MDK} when V_{MDK} is maximum dark signal voltage.



Note 9: DC signal output voltage is defined as follows. Reset noise voltage is defined as follows.



Note 10: Random noise is defined as the standard deviation (sigma) of the output level difference between two adjacent effective pixels under no illumination (i.e. dark conditions) calculated by the following procedure.



(1) Two adjacent pixels (pixel n and n + 1) after reference level clamp in one reading are fixed as measurement points.
(2) Each of the output level at video output periods averaged over 200 ns period to get V (n) and V (n + 1).
(3) V (n + 1) is subtracted from V (n) to get ΔV.

$$\Delta V = V(n) - V(n+1)$$

(4) The standard deviation of ΔV is calculated after procedure (2) and (3) are repeated 30 times (30 readings).

$$\overline{\Delta V} = \frac{1}{30}\sum_{i=1}^{30}|\Delta V_i| \qquad \sigma = \sqrt{\frac{1}{30}\sum_{i=1}^{30}\left(|\Delta V_i| - \overline{\Delta V}\right)^2}$$

(5) Procedure (2), (3) and (4) are repeated 10 times to get sigma value.
(6) 10 sigma values are averaged.

$$\bar{\sigma} = \frac{1}{10}\sum_{j=1}^{10}\sigma_j$$

(7) $\bar{\sigma}$ value calculated using the above procedure is observed $\sqrt{2}$ times larger than that measured relative to the ground level. So we specify random noise as follows.

$$ND\sigma = \frac{1}{\sqrt{2}}\bar{\sigma}$$

Operating Condition

For best performance, the device should be used within the Recommended Operating Conditions.

Characteristics		Symbol	Min	Typ.	Max	Unit
Clock pulse voltage	"H" level	$V_{\phi A}$	4.5	5.0	5.5	V
	"L" level		0	0	0.3	
Final stage clock pulse voltage	"H" level	$V_{\phi B}$	4.5	5.0	5.5	V
	"L" level		0	0	0.3	
Storage pulse voltage	"H" level	V_{ST}	2.7	3.3	5.5	V
	"L" level		0	0	0.8	
Shift pulse voltage	"H" level	V_{SH}	2.7	3.3	5.5	V
	"L" level		0	0	0.8	
Reset pulse voltage	"H" level	V_{RS}	4.5	5.0	5.5	V
	"L" level		0	0	0.5	
Switch pulse voltage	"H" level	$V_{\overline{SW}}$	2.7	3.3	5.5	V
	"L" level		0	0	0.8	
Power supply voltage		V_{OD}	11.4	12.0	12.6	V

Clock Characteristics (Ta = 25°C)

For best performance, the device should be used within the Recommended Operating Conditions.

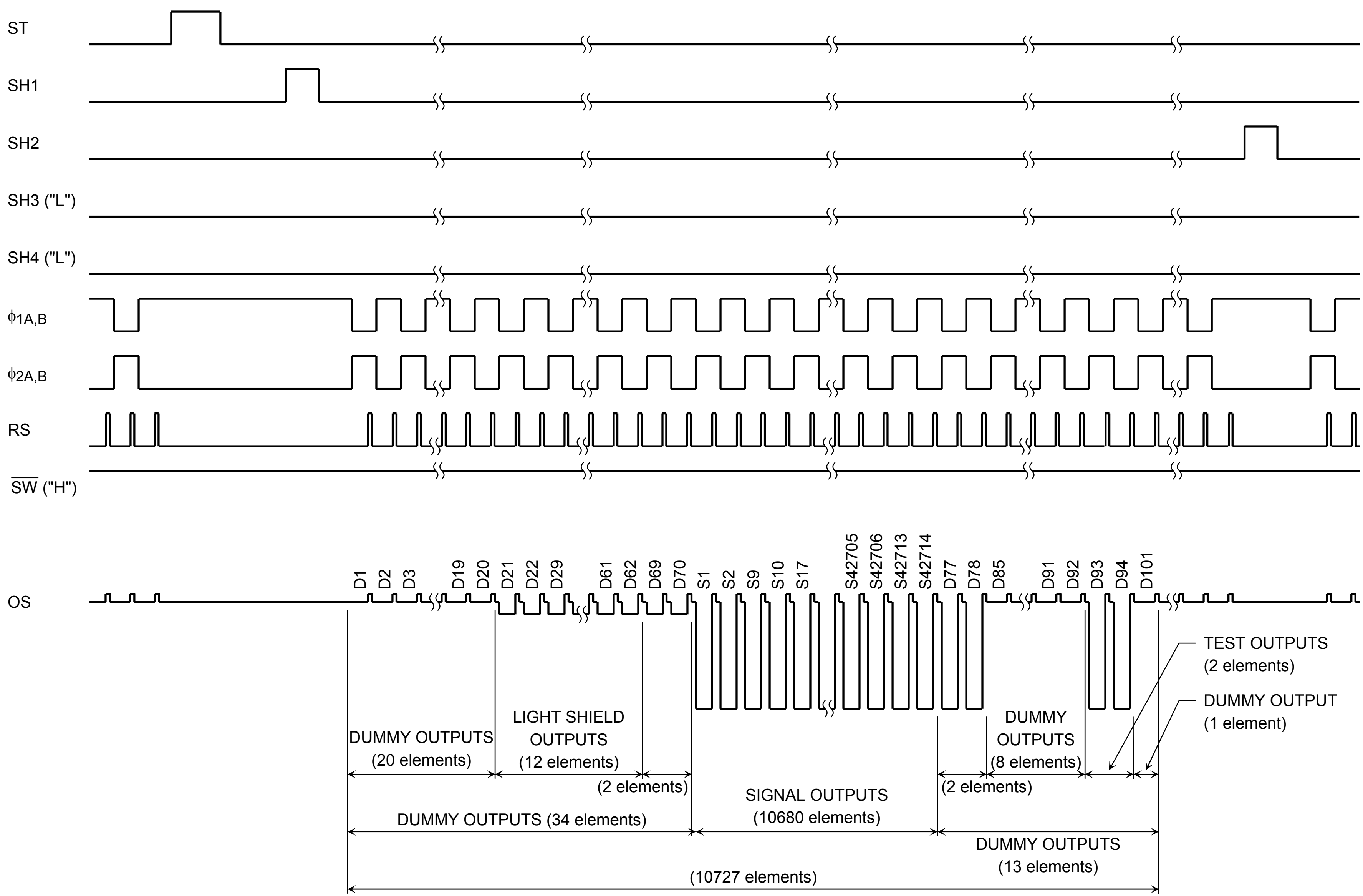
Characteristics	Symbol	Min	Typ.	Max	Unit
Clock pulse frequency	f_{ϕ}	0.15	1.0	11.0	MHz
Reset pulse frequency	f_{RS}	0.3	2.0	10.0	MHz
Clock capacitance (Note 11)	$C_{\phi A}$	—	225	—	pF
Final Stage Clock capacitance	$C_{\phi B}$	—	10	—	pF
Storage gate capacitance	C_{ST}	—	30	—	pF
Shift gate capacitance	C_{SH}	—	30	—	pF
Reset gate capacitance	C_{RS}	—	20	—	pF
Switch gate capacitance	$C_{\overline{SW}}$	—	10	—	pF

Note 11: V_{OD} = 12 V

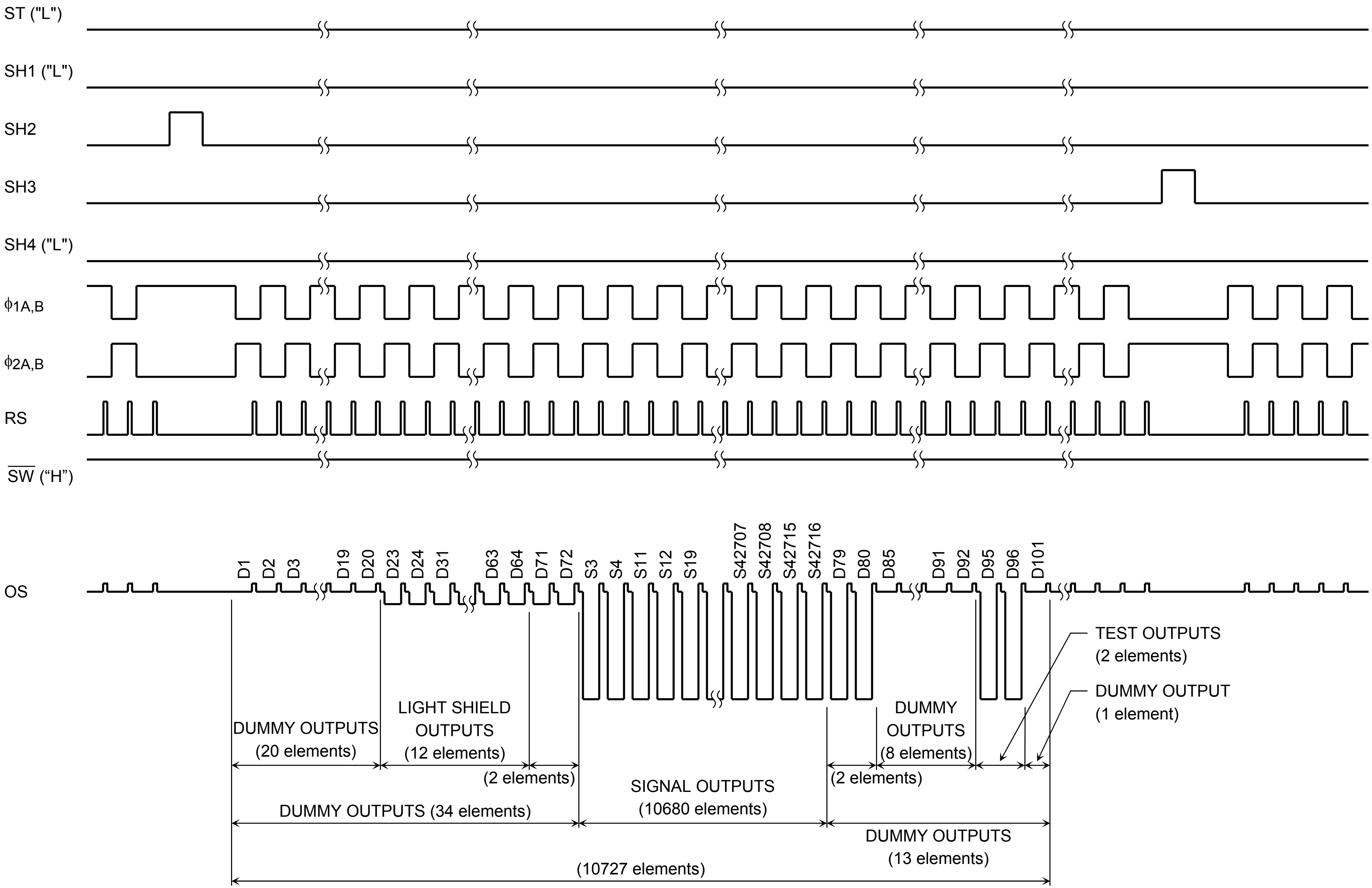
Mode Select

$\overline{SW}$	Mode
H	4800dpi mode
L	2400dpi mode 1200dpi mode 600dpi mode

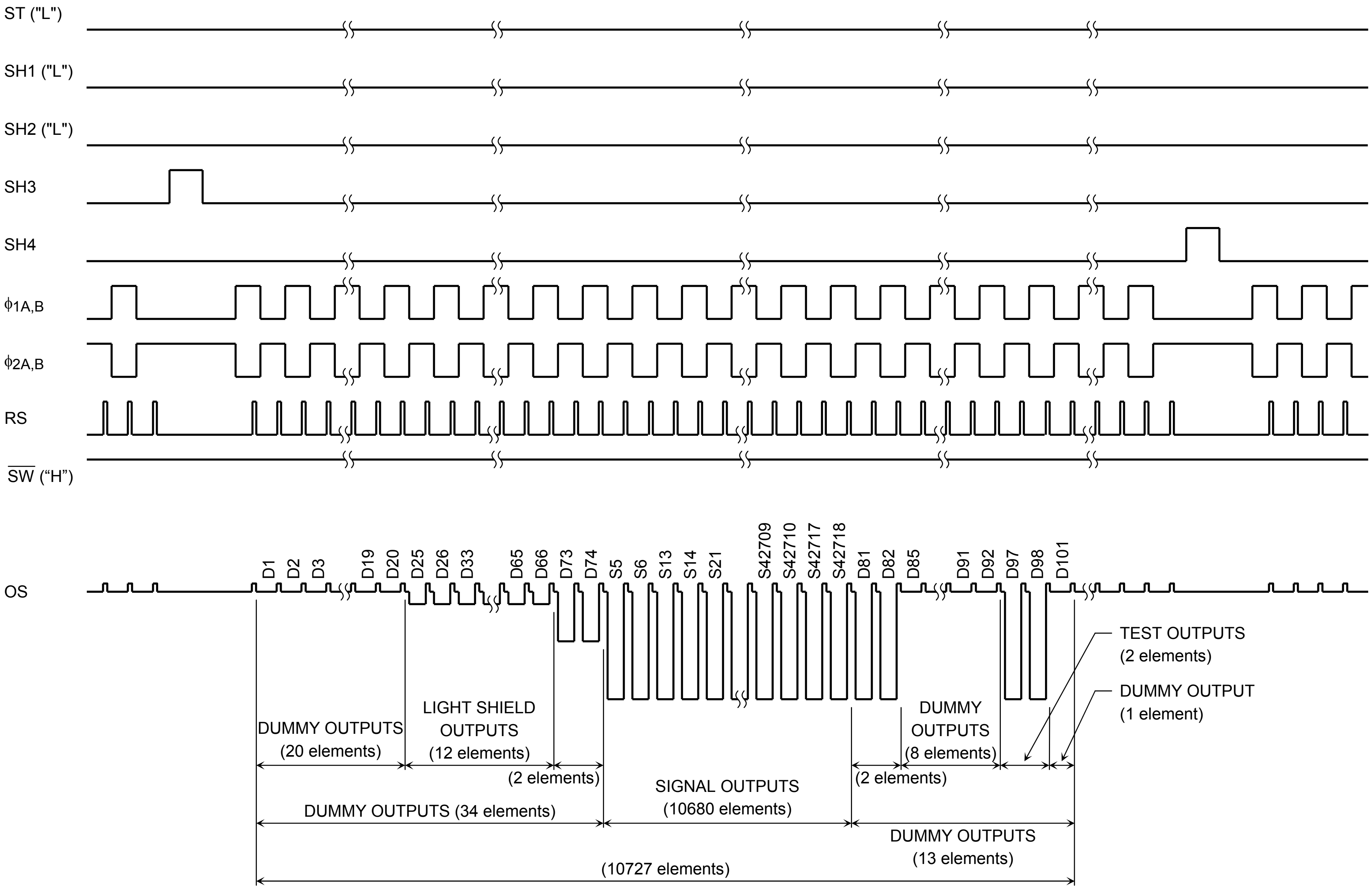
Timing Chart 1 (4800DPI mode (1))



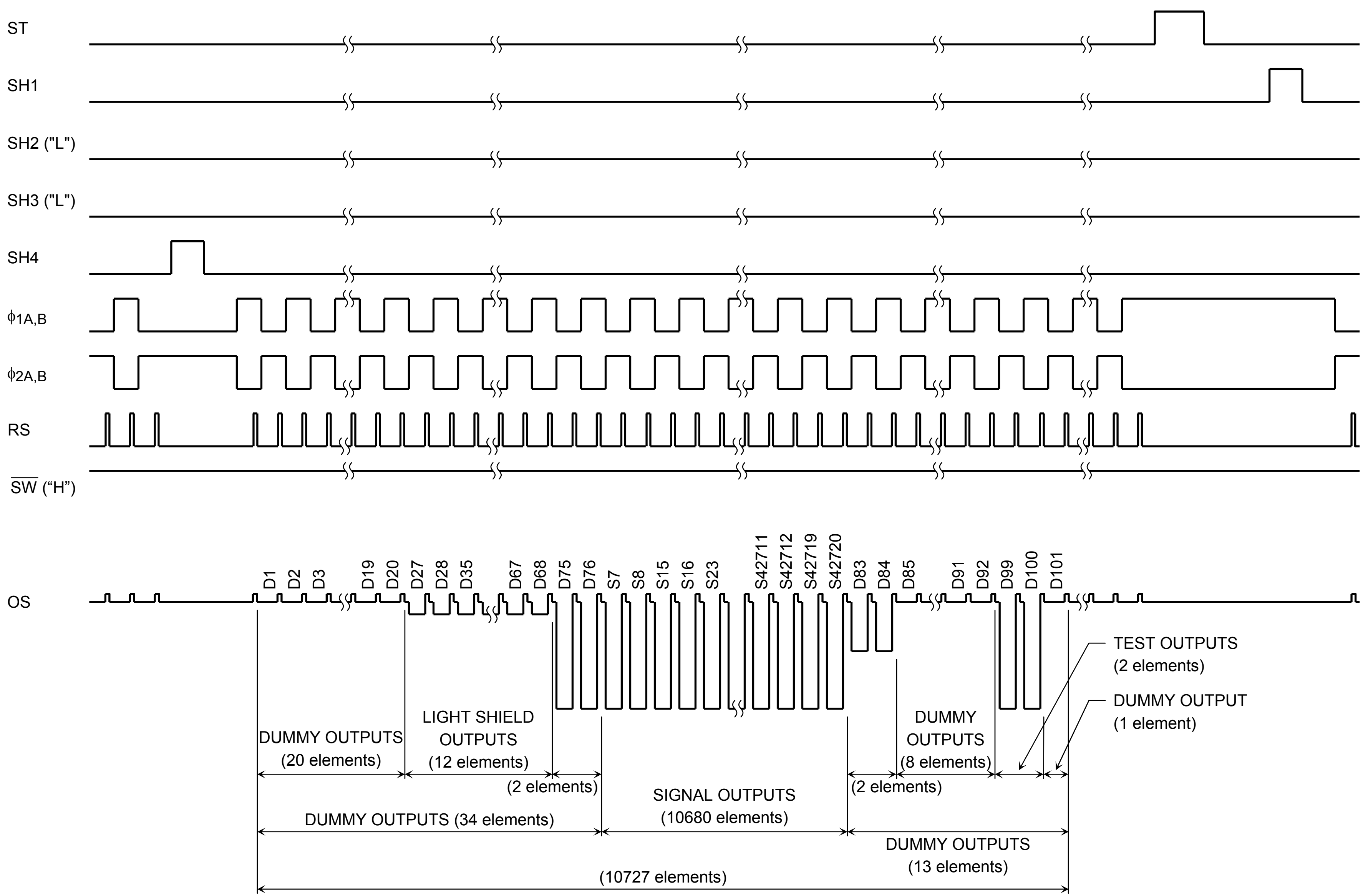
Timing Chart 2 (4800DPI mode (2))



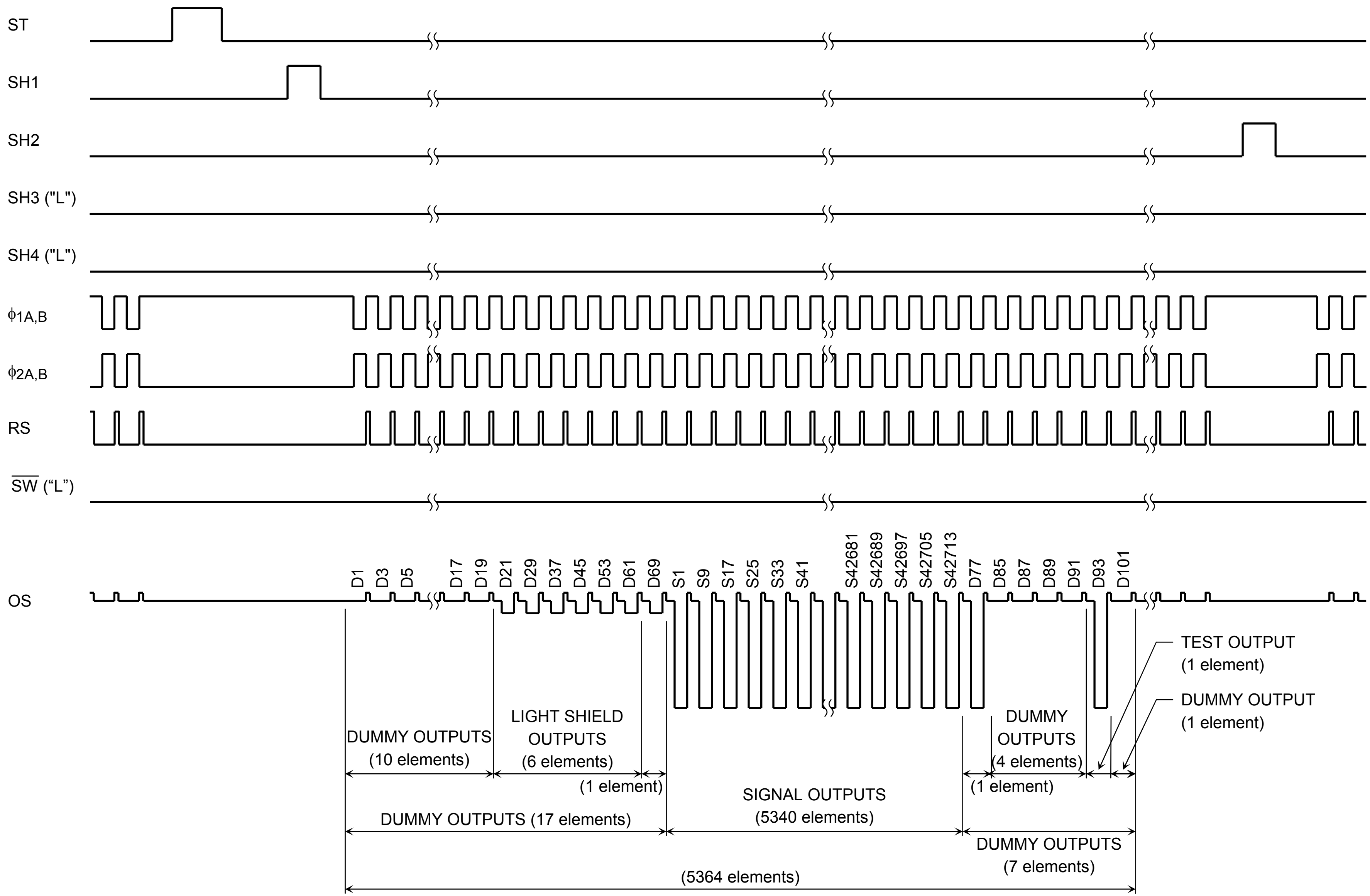
Timing Chart 3 (4800DPI mode (3))



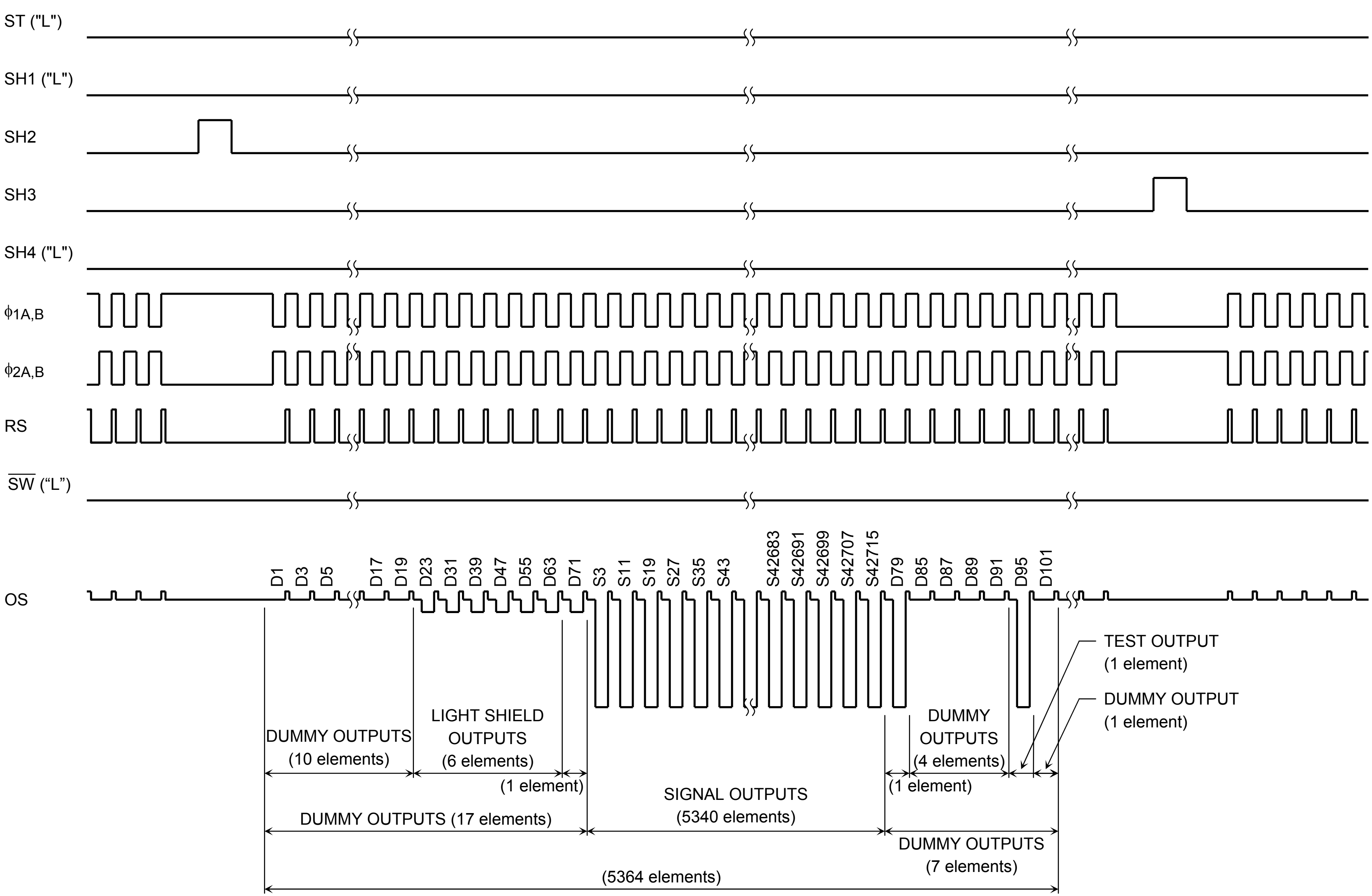
Timing Chart 4 (4800DPI mode (4))



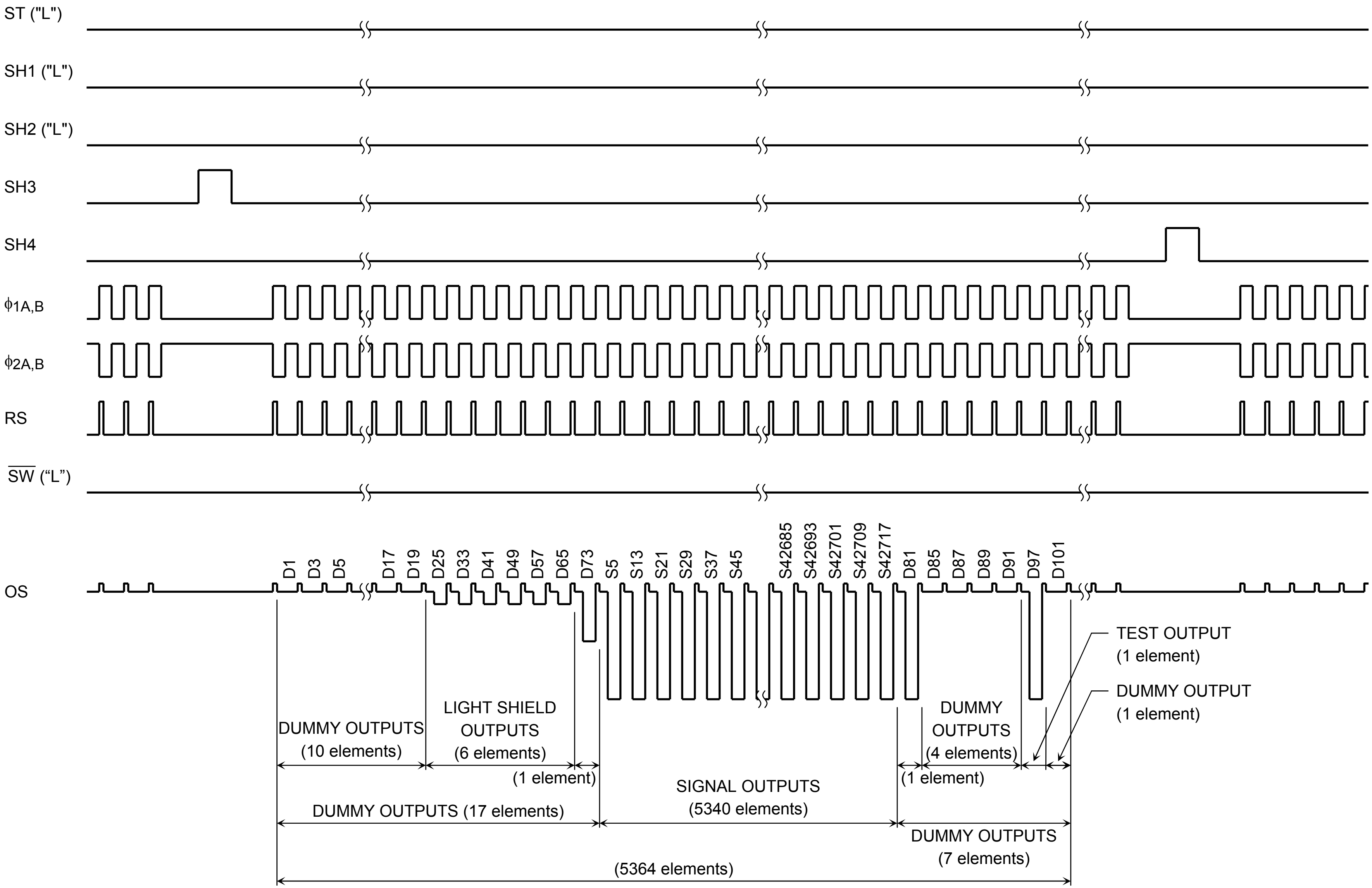
Timing Chart 5 (2400DPI mode (1))



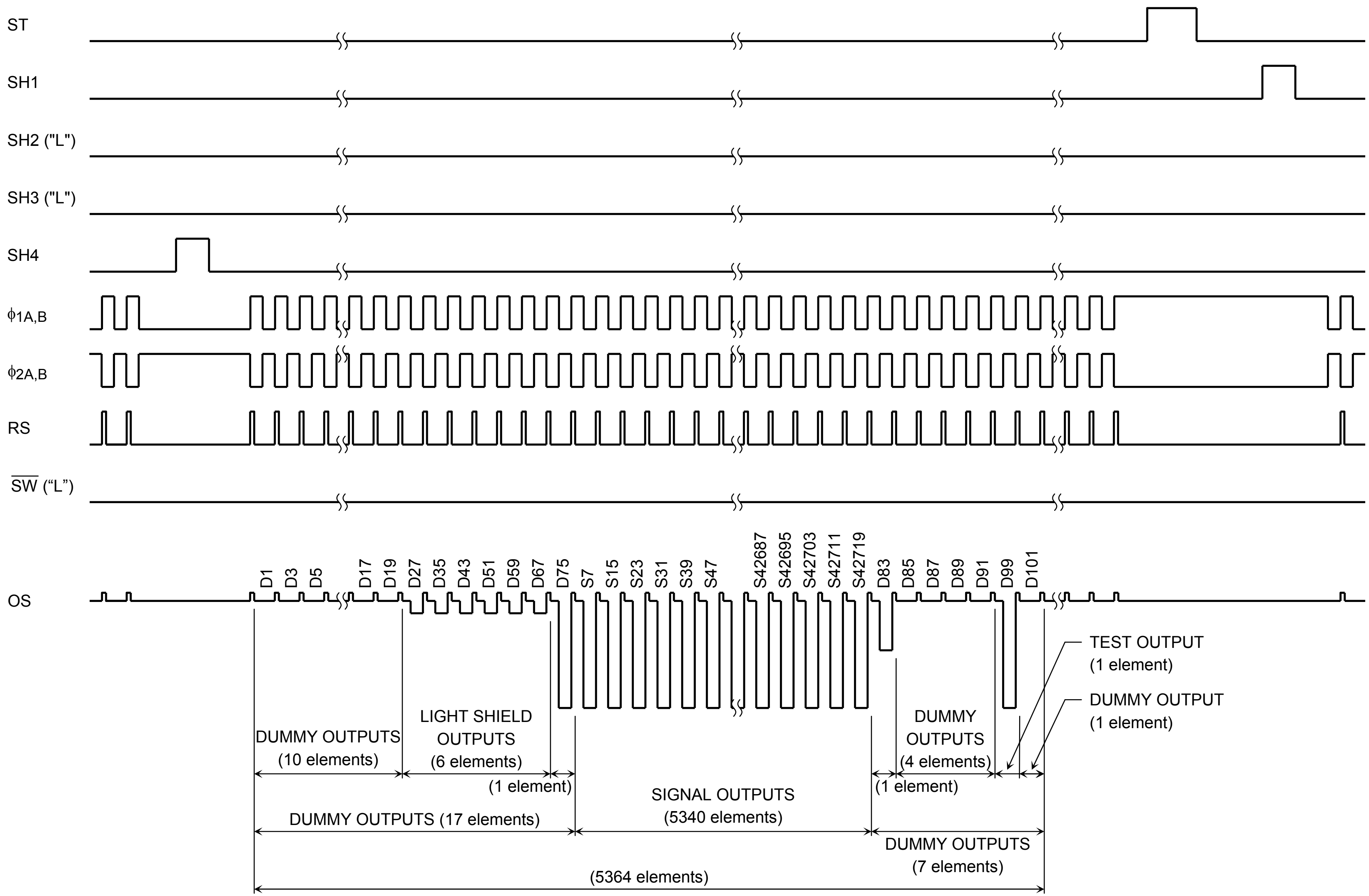
Timing Chart 6 (2400DPI mode (2))



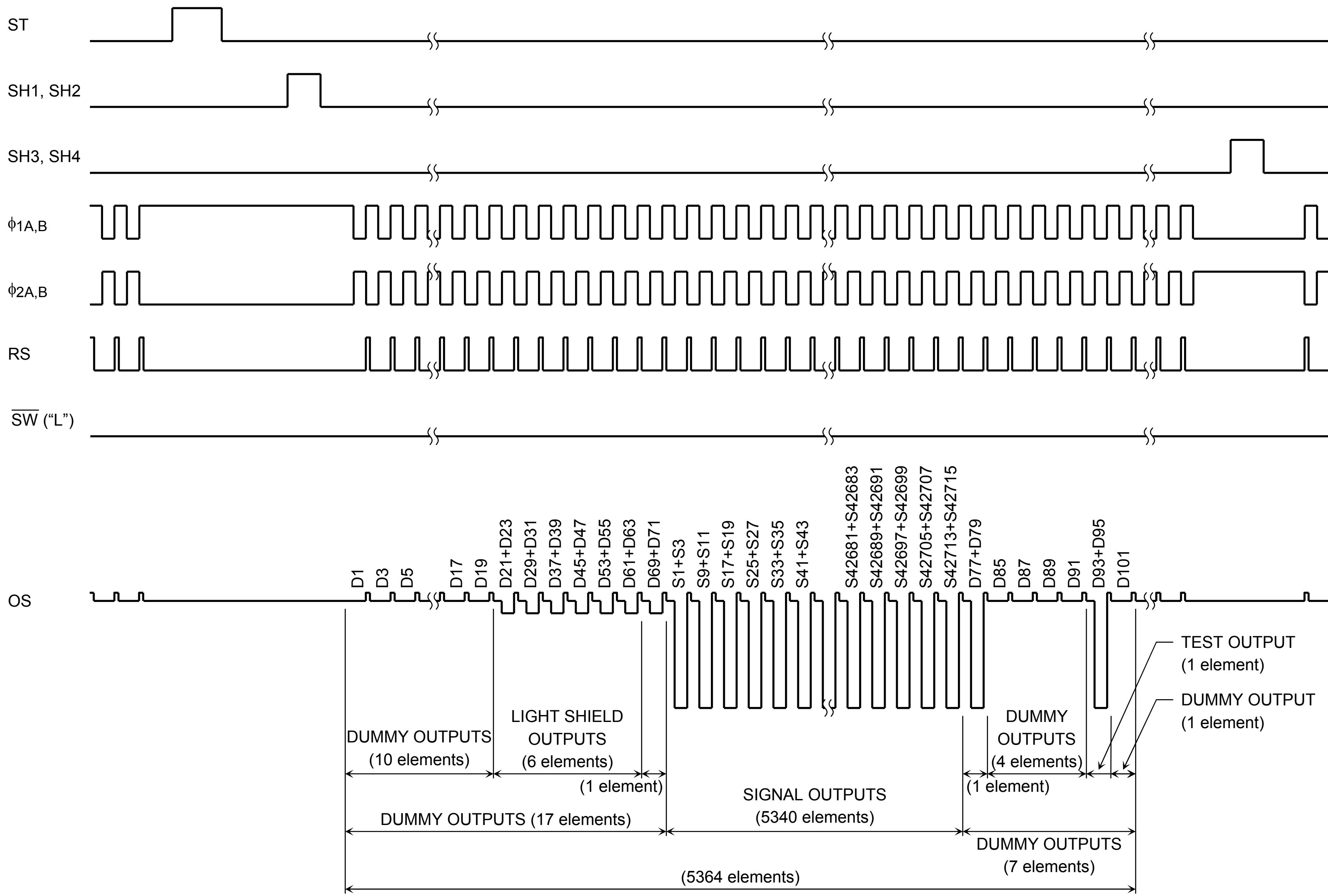
Timing Chart 7 (2400DPI mode (3))



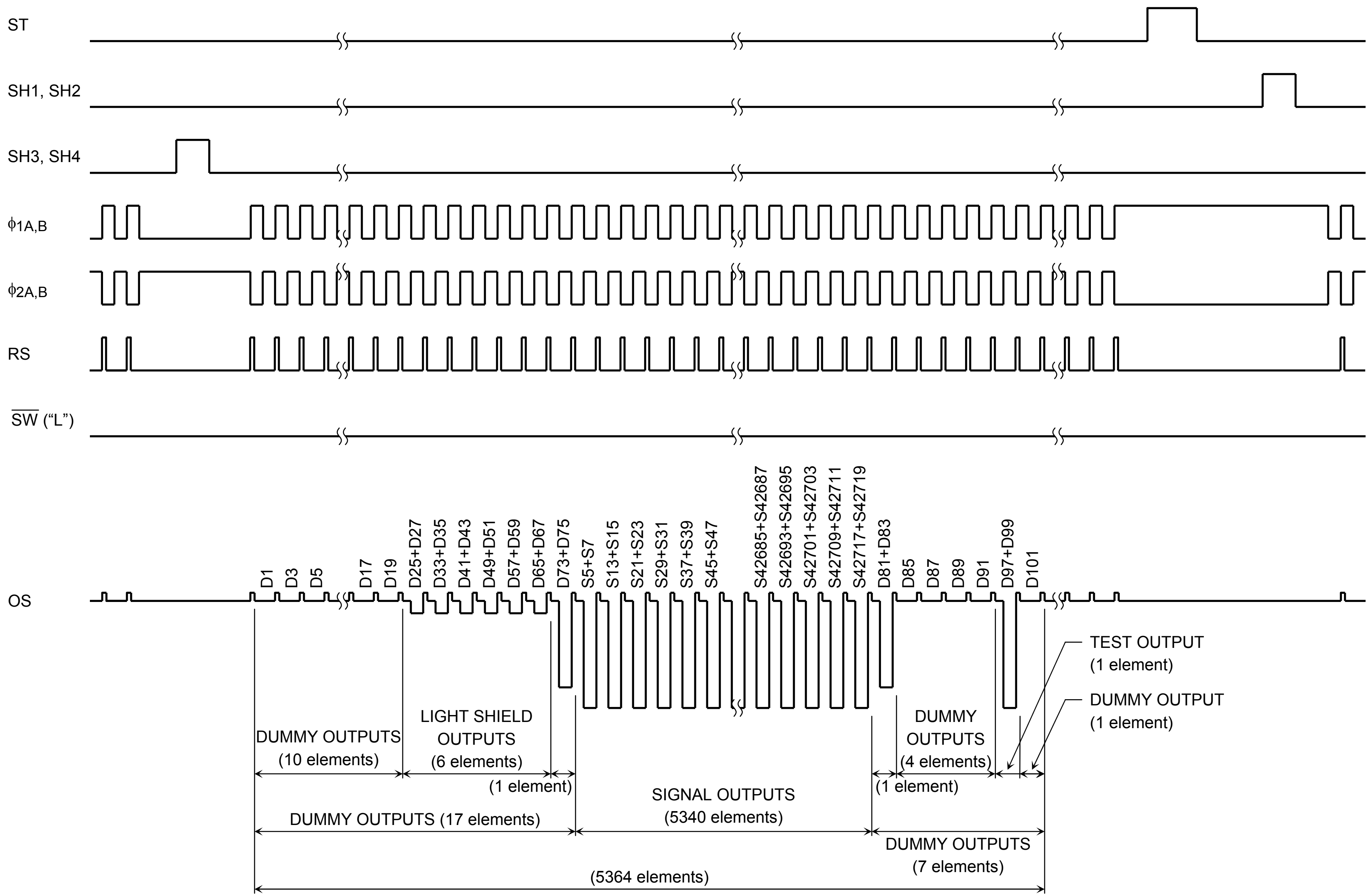
Timing Chart 8 (2400DPI mode (4))



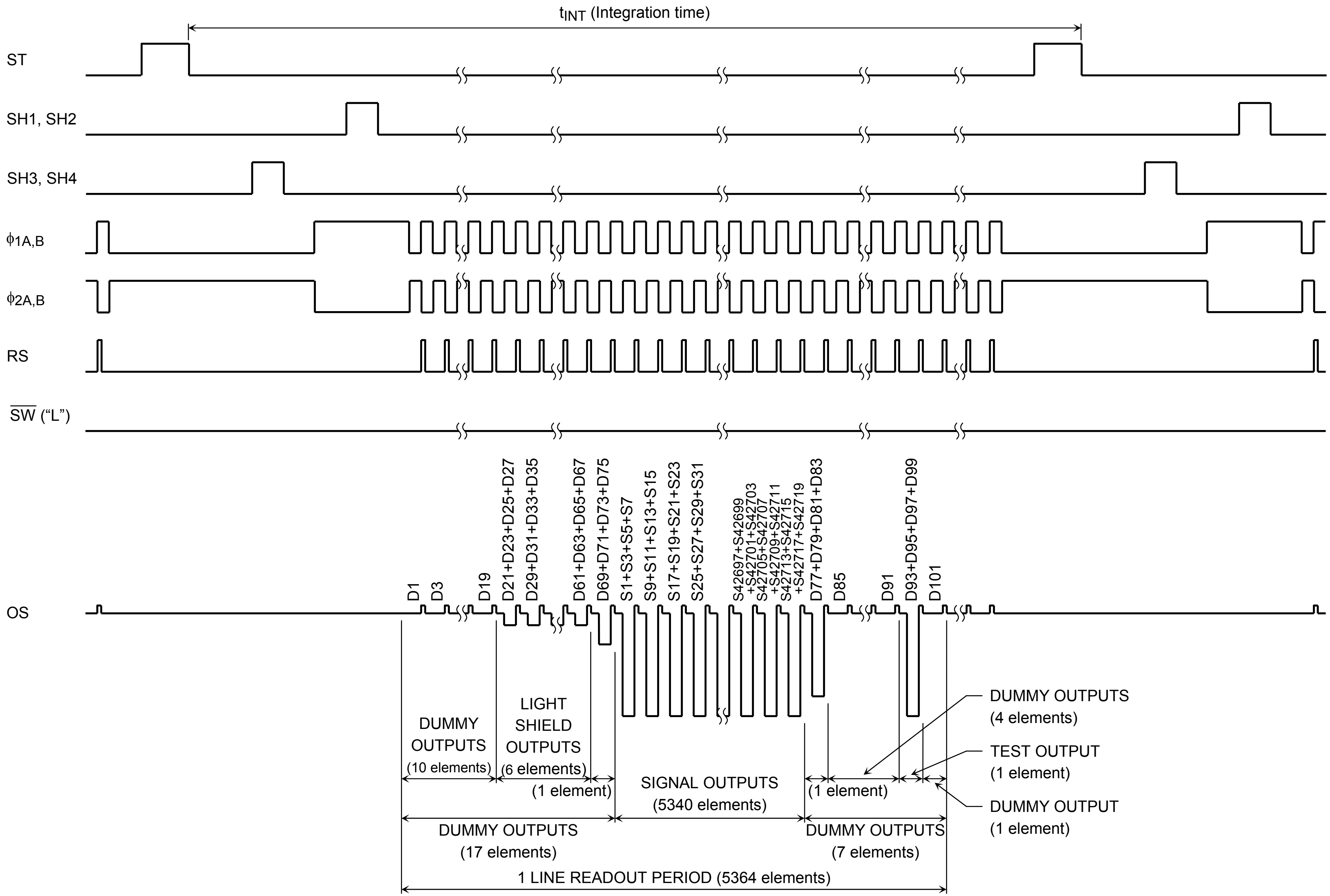
Timing Chart 9 (1200DPI mode (1))



Timing Chart 10 (1200DPI mode (2))

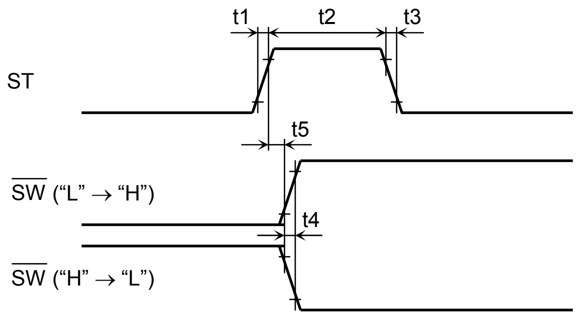


Timing Chart 11 (600DPI mode)

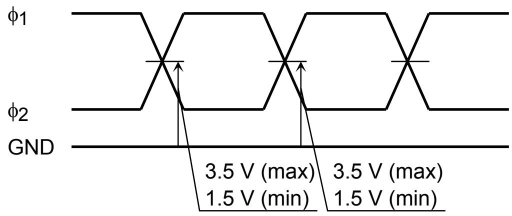


Timing Requirements

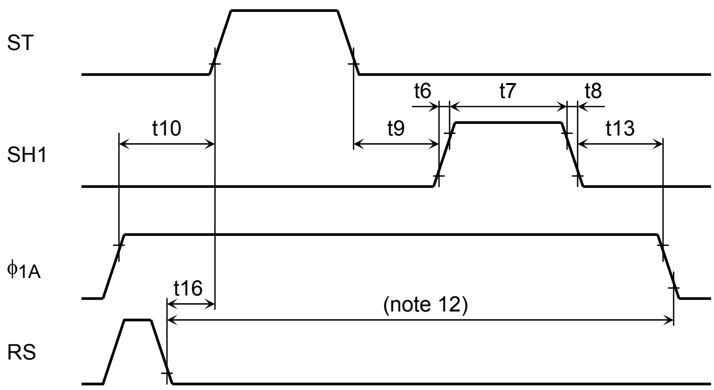
ST, $\overline{SW}$ Timing



φ1, φ2 Cross point

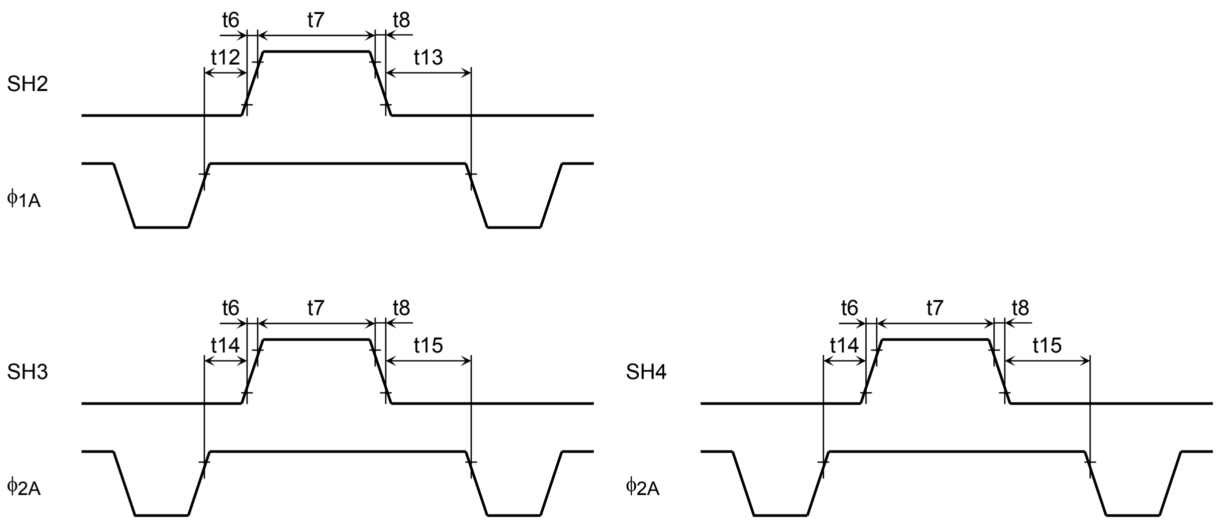


ST, SH, φ1A, RS Timing (4800DPI / 2400DPI Mode)

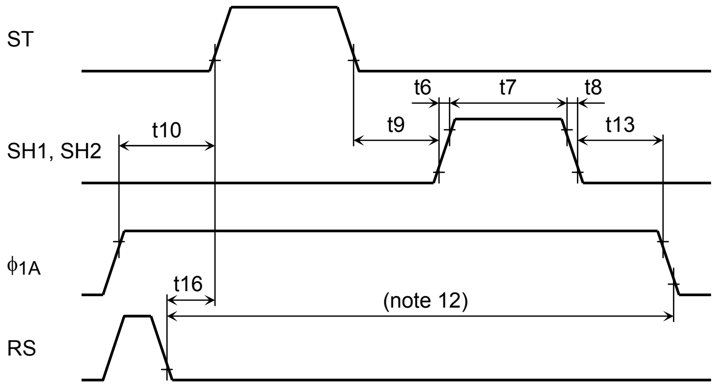


Note 12: Set the voltage level of RS to “L” level.

SH, φ1A, φ2A Timing (4800DPI / 2400DPI Mode)

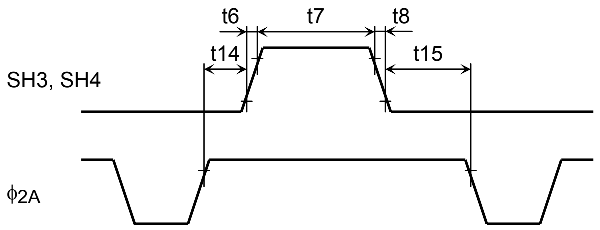


ST, SH, ϕ1A, RS Timing (1200DPI Mode)

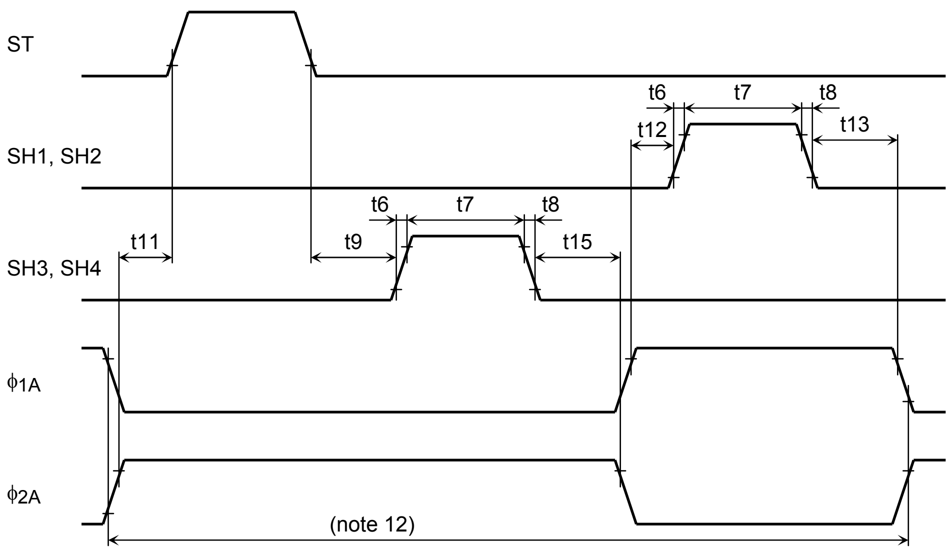


Note 12: Set the voltage level of RS to “L” level.

SH, ϕ2A Timing (1200DPI Mode)

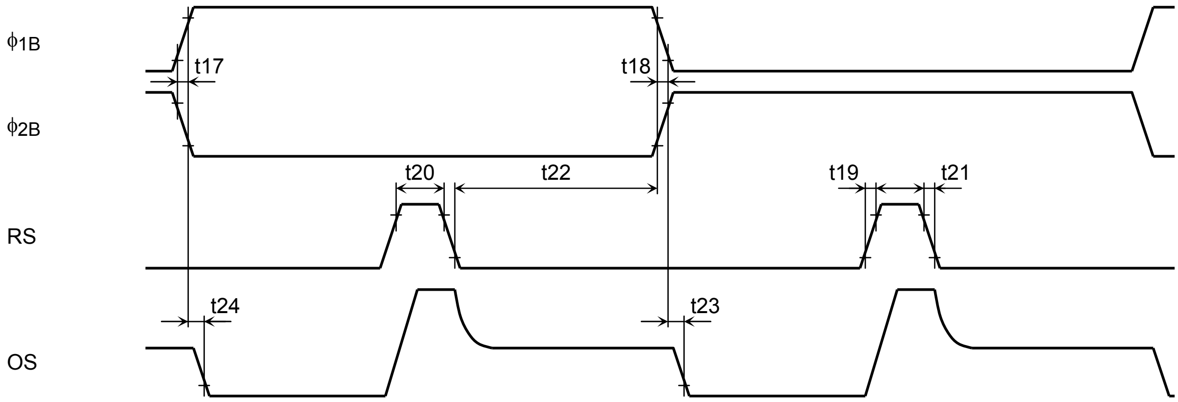


ST, SH, ϕ1A, ϕ2A Timing (600DPI Mode)

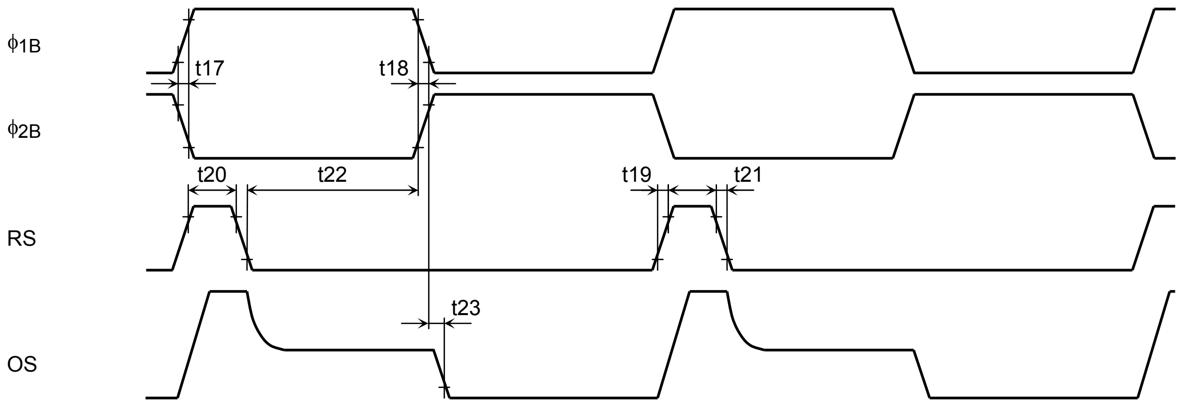


Note 12: Set the voltage level of RS to “L” level.

ϕ1, ϕ2, RS, OS Timing (4800DPI Mode)



ϕ1, ϕ2, RS, OS Timing (2400DPI / 1200DPI / 600DPI Mode)



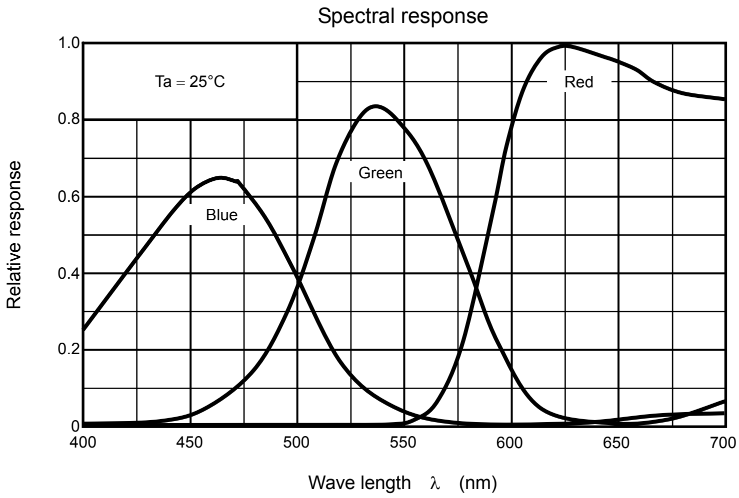
Timing Requirements

Characteristics	Symbol	Min	Typ. (Note 13)	Max	Unit
ST pulse rise time, fall time	t1, t3	0	50	—	ns
ST pulse width	t2	3000	5000	—	ns
$\overline{SW}$ pulse rise time, fall time	t4	0	50	—	ns
Pulse timing of ST and $\overline{SW}$	t5	0	0	—	ns
SH pulse rise time, fall time	t6, t8	0	50	—	ns
SH pulse rise width	t7	3000	5000	—	ns
Pulse timing of ST and SH	t9	3000	5000	—	ns
Pulse timing of ST and ϕ_{1A}	t10	110	1000	—	ns
Pulse timing of ST and ϕ_{2A}	t11	110	1000	—	ns
Pulse timing of SH and ϕ_{1A}	t12	110	1000	—	ns
	t13	3000	5000	—	ns
Pulse timing of SH and ϕ_{2A}	t14	110	1000	—	ns
	t15	3000	5000	—	ns
Pulse timing of ST and RS	t16	0	500	—	ns
ϕ_1, ϕ_2 pulse rise time, fall time	t17, t18	0	50	—	ns
RS pulse rise time, fall time	t19, t21	0	20	—	ns
RS pulse width	t20	15	100	—	ns
Pulse timing of ϕ_{1B}, ϕ_{2B} and RS	t22	10	50	—	ns
Video data delay time (Note 14)	t23, t24	—	25	—	ns

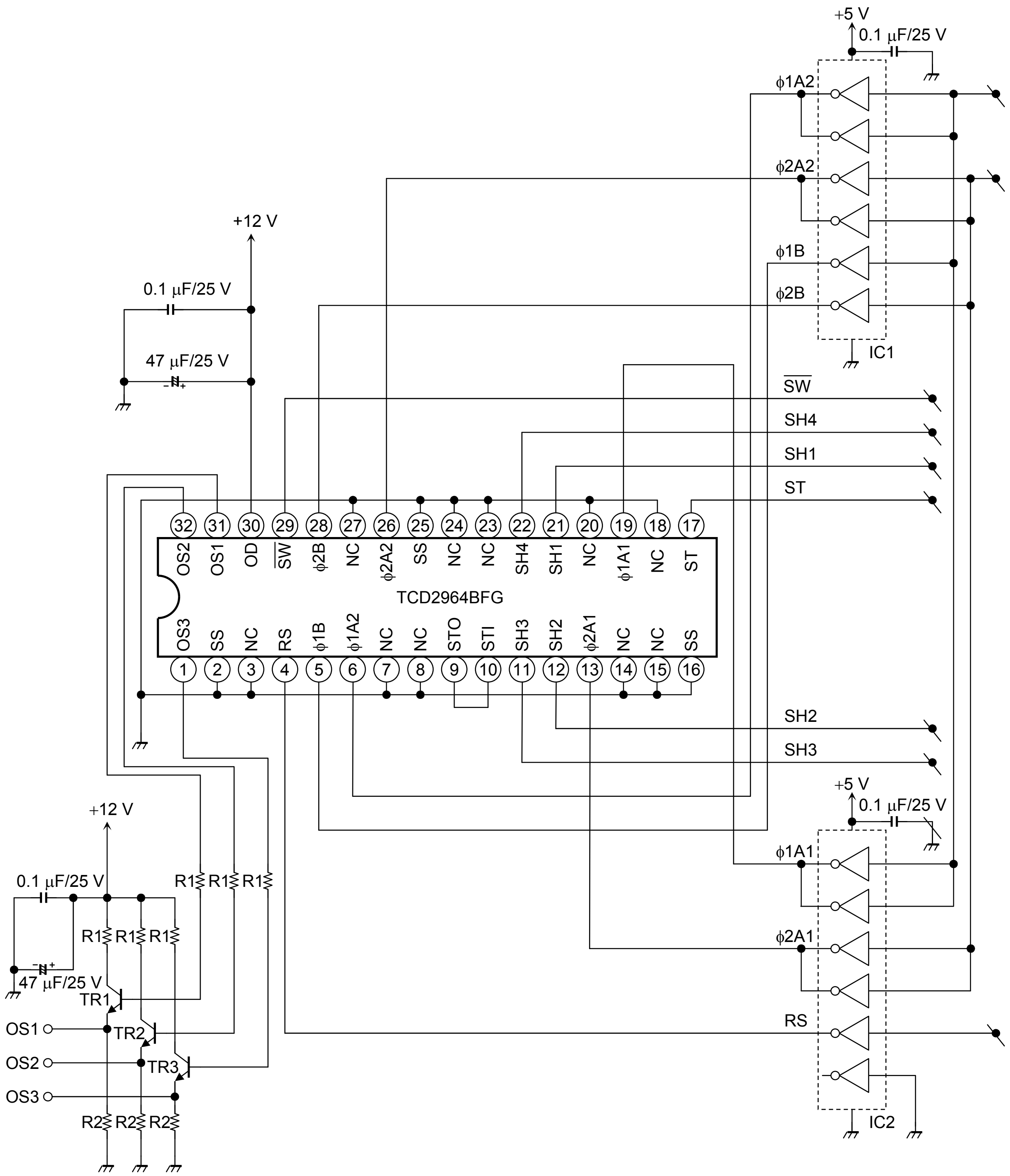
Note 13: Typ. is the case of fϕ = 1.0 MHz.

Note 14: Load resistance is 100 kΩ.

Typical Spectral Response



Typical Drive Circuit



IC1, 2: TC74AC04P
TR1, 2, 3: 2SC1815-Y
R1: 150 Ω
R2: 1500 Ω

Caution

1. Electrostatic Breakdown

Store in shorting clip or in conductive foam to avoid electrostatic breakdown.

CCD Image Sensor is protected against static electricity, but inferior puncture mode device due to static electricity is sometimes detected. In handing the device, it is necessary to execute the following static electricity preventive measures, in order to prevent the trouble rate increase of the manufacturing system due to static electricity.

a. Prevent the generation of static electricity due to friction by making the work with bare hands or by putting on cotton gloves and non-charging working clothes.
b. Discharge the static electricity by providing earth plate or earth wire on the floor, door or stand of the work room.
c. Ground the tools such as soldering iron, radio cutting pliers of or pincer.
   It is not necessarily required to execute all precaution items for static electricity.
   It is all right to mitigate the precautions by confirming that the trouble rate within the prescribed range.
d. Ionized air is recommended for discharge when handling CCD image sensors.

2. Incident Light

CCD sensor is sensitive to infrared light. Note that infrared light component degrades resolution and PRNU of CCD sensor.

3. Cloudiness of Glass Inside

CCD surface mount products may have a haze on the inside of glass, so be careful about following. Even if the haze arises inside of glass, when it is not on the pixel area, there is no problem in quality.

a. Before the aluminum bag is opened, please keep the products in the environment below 30°C90%RH. And after the aluminum bag is opened, please keep the products in the environment below 30°C60%RH .
b. Please mount the products within 12month from sealed date and within 6 month from opening the aluminum bag. (Sealed date is printed on aluminum bag.)

4. Ultrasonic Cleaning

Ultrasonic cleaning should not be used with such hermetically-sealed ceramic package as CCD because the bonding wires can become disconnected due to resonance during the cleaning process.

5. Mounting

In the case of solder mounting, the devices should be mounted with the window glass protective tape in order to avoid dust or dirt included in reflow machine.

6. Window Glass Protective Tape

The window glass protective tape is manufactured from materials in which static charges tend to build up. When removing the tape from CCD sensor after solder mounting, install an ionizer to prevent the tape from being charged with static electricity.

When the tape is removed, adhesives will remain in the glass surface. Since these adhesives appear as black or white flaws on the image, please wipe the window glass surface with the cloth into which the organic solvent was infiltrated. Then please attach CCD to a product.

Do not reuse the tape.

7. Soldering Temperature Profile for Pb free

Good temperature profile for each soldering method is as follows. In addition, in case of the repair work accompanied by IC removal, since the degree of parallel may be spoiled with the left solder, please do not carry out and in case of the repair work not accompanied by IC removal, carry out with a soldering iron or , in reflow, only one time.

a. Using a soldering iron
Complete soldering within ten seconds for lead temperatures of up to 260°C, or within three seconds for lead temperatures of up to 350°C.

b. Using long infrared rays reflow / hot air reflow
Please do reflow at the condition that the package surface (electrode) temperature is on the solder maker's recommendation profile. And that reflow profile is within below condition 1 to 3.

1. Peak temperature: 250°C or less.
2. Time to keep high temperature : 220~250°C, 30~40sec.
3. Pre. heat : 150~190°C, 60~120sec

8. Window Glass

The dust and stain on the glass window of the package degrade optical performance of CCD sensor.

Keep the glass window clean by saturating a cotton swab in alcohol and lightly wiping the surface, and allow the glass to dry, by blowing with filtered dry N2. Care should be taken to avoid mechanical or thermal shock because the glass window is easily to damage.

9. Cleaning Method of the Window Glass Surface

Wiping Cloth

a. Use soft cloth with a fine mesh.
b. The wiping cloth must not cause dust from itself.
c. Use a clean wiping cloth necessarily.

Recommended wiping cloth is as follow;
- MK cloth (Toray Industries)

Cleaner

Recommended cleaning liquid of window glass are as follow;
- EE-3310 (Olympus)

When using solvents, such as alcohol, unavoidably, it is cautious of the next.

a. A clean thing with quick-drying.
b. After liquid dries, there needs to be no residual substance.
c. A thing safe for a human body.

And, please observe the use term of a solvent and use the storage container of a solvent to be clean.

Be cautious of fire enough.

Way of Cleaning

First, the surface of window glass is wiped with the wiping cloth into which the cleaner was infiltrated. Please wipe down the surface of window glass at least 2 times or more.

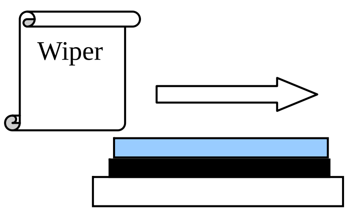
Next, the surface of window glass wipes with the dry wiping cloth. Please wipe down the surface of window glass at least 3 times or more.

Finally, blow cleaning is performed by dry N2 filtered.

If operator wipes the surface of the window glass with the above-mentioned process and dirt still remains, Toshiba recommends repeating the clean operation from the beginning.

Be cautious of the next thing.

a. Don't infiltrate the cleaner too much.
b. A wiping portion is performed into the optical range and don't touch the edge of window glass.
c. Be sure to wipe in a long direction and the same direction.
d. A wiping cloth always uses an unused portion.



10. Foot Pattern on the PCB

We recommend fig1's foot pattern for your PCB(Printed circuit Board).

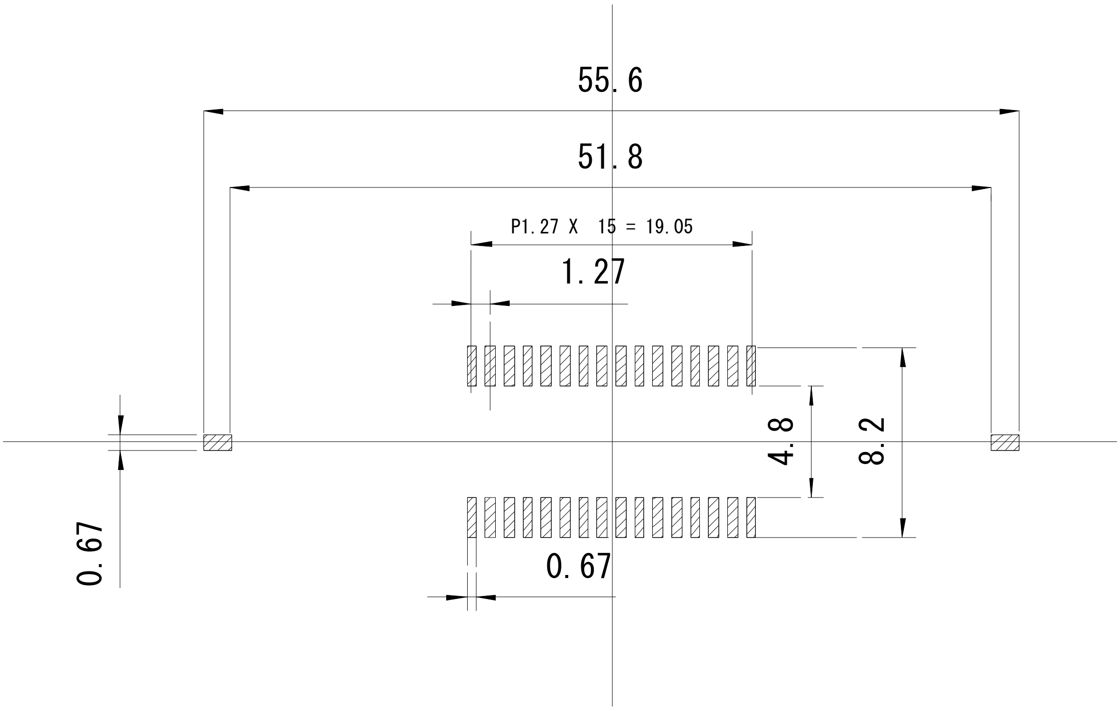


fig1

11. Mask for Solder Paste Application

We recommend metal mask that have the following thickness.
- TCD****BFG(Pad material : Au) : a thickness of 0.2mm.

And we recommend that the size of the pattern of the metal mask is 95% to 100% of recommended foot pattern at fig1.

12. Temperature cycle

After mounting, if temperature cycle stress is too much, CCD surface mount products have a possibility that a crack may arise in solder. As a method of preventing a solder crack, underfil is effective

13. Reuse of a Tray

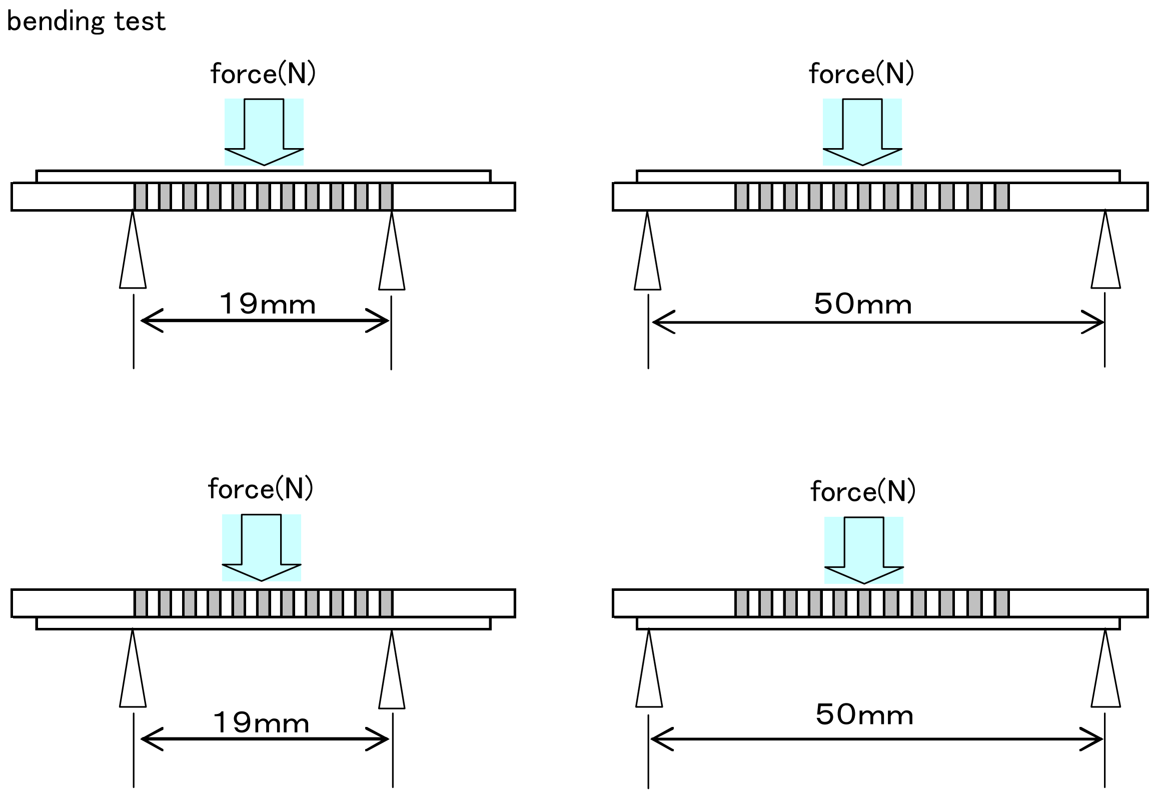
We reuse tray in order to reduce plastic waste as we can. Please cooperate with us in reusing for ecology.

14. Caution for Package Handling

Over force on CCD products may cause crack and chip removing on the product. The three point bending strength of this product is the following. (Reference data)

If the stress is loaded far from a fulcrum, the stress on the package will be increase.

When you will treat CCD on every process, please be careful particularly. For example, soldering on PCB, cutting PCB, wiping on the glass surface, optical assemble and so on.



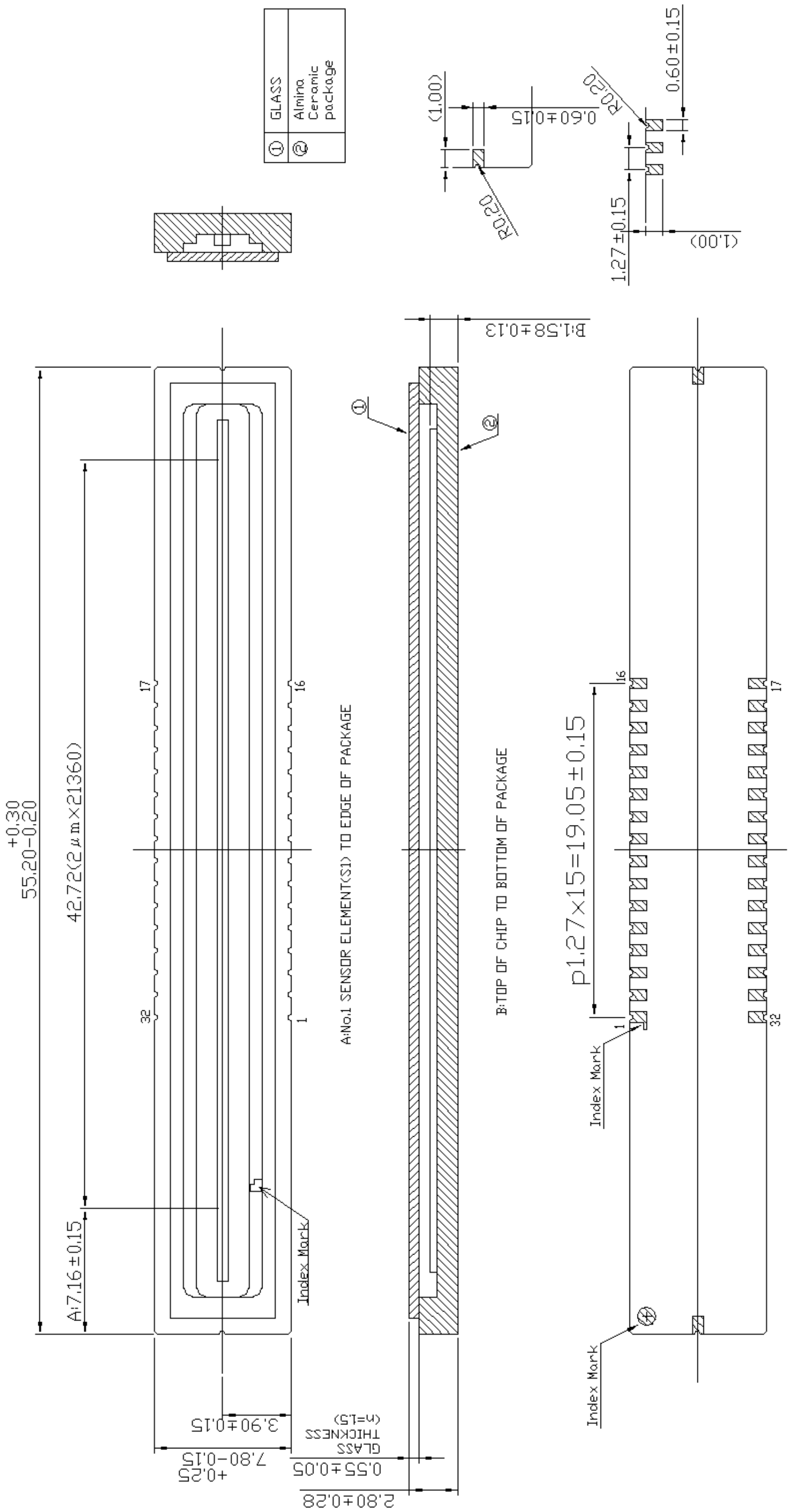
- 32CLCC

Bearing length 19mm :	The force from upside : 250[N]
	The force from downside : 150[N]
Bearing length 50mm :	The force from upside : 120[N]
	The force from downside : 60[N]

15. Dummy Scan

The device cannot output normal signal immediately after power-on. Execute 20lines of dummy scan to obtain normal signal output.

Package Dimensions



Weight: 3.2 g (typ.)

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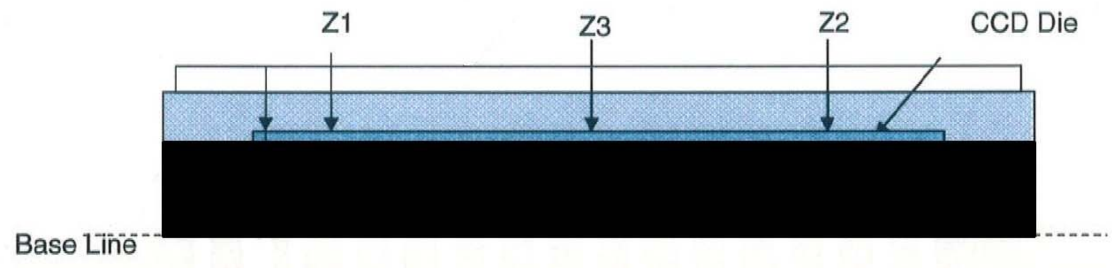
Overflow Drain Performance

Specified as below.
No blooming when exposed 4.45 times the exposure that gives 2.4V of output voltage at tINT=22ms and exposed area on CCD=9.6mm.

Chip Warpage

Specified as 0 +/− 20 [um] by the definition below. This specification is based on the actual distribution. No inspection is performed for the products.
(Definition)
In the figure below, chip warpage is defined as the vertical distance of Z3 from the line connecting Z1 and Z2 (datum).
When Z3 is at cover glass side from the datum, the sign is defined as "+".
When Z3 is at package side from the datum, the sign is defined as "−".
Chip warpage is defined by the product before solder mounting on PCB.



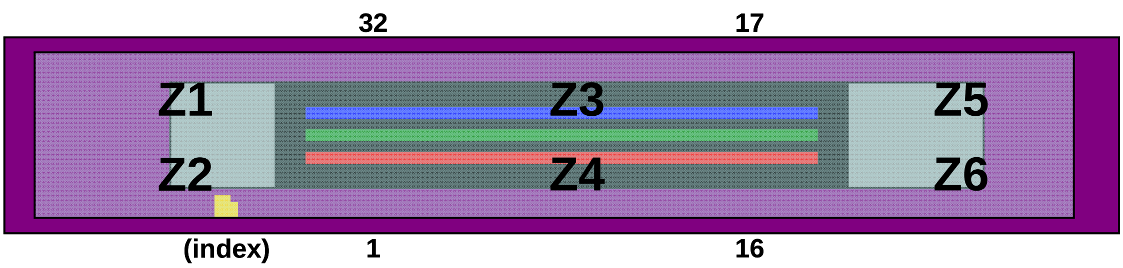
Chip Slope

Specified as follows by the definition below.
0 +/− 0.25 [degree] for longer direction
0 +/− 2 [degree] for shorter direction
This specification is based on the actual distribution. No inspection is performed for the products.
(Definition)
In the figure below, chip slope is calculated by Z1, Z2, ・・・, Z6 value from bottom of package.

for longer direction; Chip slope is defined by Z1 and Z5 and by Z2 and Z6.
When Z5>Z1 or Z6>Z2, the sign is defined as "+".
When Z5<Z1 or Z6<Z2, the sign is defined as "−".

for shorter direction; Chip slope is defined by Z1 and Z2, by Z3 and Z4 and by Z5 and Z6.
When Z1>Z2 or Z3>Z4 or Z5>Z6, the sign is defined as "+".
When Z1<Z2 or Z3<Z4 or Z5<Z6, the sign is defined as "−".

Chip slope is defined by the product before solder mounting on PCB.



Change history

Rev.	Date	Description
0	2009-09-15	New
1	2015-11-12	changed warning ABSOLUTE MAXIMUM RATINGS, Operating Condition, Clock Characteristics
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