LM393, LM393E, LM293, LM2903, LM2903E, LM2903V, NCV2903

Low Offset Voltage Dual Comparators

The LM393 series are dual independent precision voltage comparators capable of single or split supply operation. These devices are designed to permit a common mode range–to–ground level with single supply operation. Input offset voltage specifications as low as 2.0 mV make this device an excellent selection for many applications in consumer, automotive, and industrial electronics.

Features

- Wide Single–Supply Range: 2.0 Vdc to 36 Vdc
- Split–Supply Range: ±1.0 Vdc to ±18 Vdc
- Very Low Current Drain Independent of Supply Voltage: 0.4 mA
- Low Input Bias Current: 25 nA
- Low Input Offset Current: 5.0 nA
- Low Input Offset Voltage: 5.0 mV (max) LM293/393
- Input Common Mode Range to Ground Level
- Differential Input Voltage Range Equal to Power Supply Voltage
- Output Voltage Compatible with DTL, ECL, TTL, MOS, and CMOS Logic Levels
- ESD Clamps on the Inputs Increase the Ruggedness of the Device without Affecting Performance
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q100 Qualified and PPAP Capable
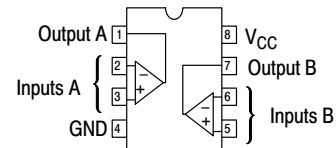- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

ON Semiconductor®
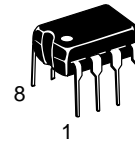
PDIP–8
N SUFFIX
CASE 626

SOIC–8
D SUFFIX
CASE 751

Micro8™
DM SUFFIX
CASE 846A

PIN CONNECTIONS

Output A 1	8 V_{CC}
Inputs A { 2 / 3	7 Output B
GND 4	6 / 5 Inputs B

(Top View)

DEVICE MARKING AND ORDERING INFORMATION

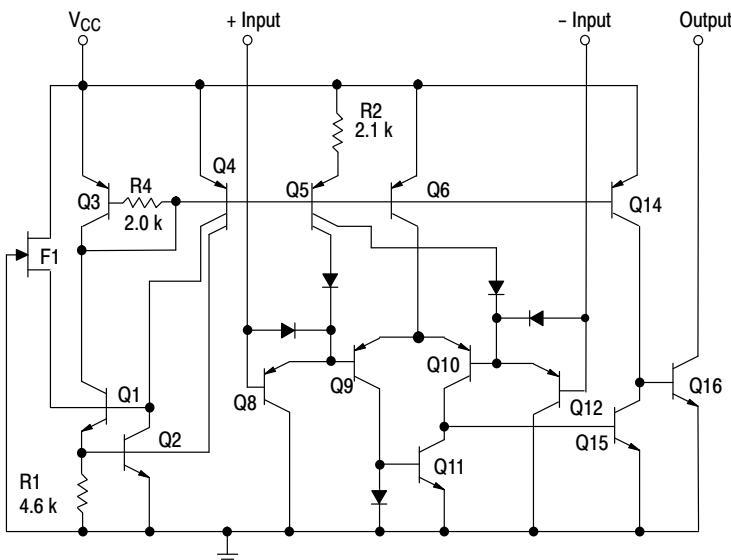See detailed marking information and ordering and shipping information on pages 6 and 7 of this data sheet.

Figure 1. Representative Schematic Diagram
(Diagram shown is for 1 comparator)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+36 or $\pm$18	V
Input Differential Voltage	V_{IDR}	36	V
Input Common Mode Voltage Range	V_{ICR}	−0.3 to +36	V
Output Voltage	V_O	36	V
Output Short Circuit–to–Ground Output Sink Current (Note 1)	I_{SC} I_{Sink}	Continuous 20	mA
Power Dissipation @ T_A = 25°C Derate above 25°C	P_D $1/R_{\theta JA}$	570 5.7	mW mW/°C

Operating Ambient Temperature Range
    LM293
    LM393, LM393E
    LM2903, LM2903E
    LM2903V, NCV2903 (Note 2)
	T_A	
		−25 to +85
		0 to +70
		−40 to +105
		−40 to +125
			°C

Maximum Operating Junction Temperature
    LM393, LM393E, LM2903, LM2903E, LM2903V
    LM293, NCV2903
	$T_{J(max)}$	
		150
		150
			°C

Storage Temperature Range	T_{stg}	−65 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. The maximum output current may be as high as 20 mA, independent of the magnitude of V_{CC}, output short circuits to V_{CC} can cause excessive heating and eventual destruction.
2. *NCV2903 is qualified for automotive use.*

ESD RATINGS

Rating	HBM	MM	Unit
ESD Protection at any Pin (Human Body Model – HBM, Machine Model – MM)			
NCV2903 (Note 2)	2000	200	V
LM393E, LM2903E	1500	150	V
LM393DG/DR2G, LM2903DG/DR2G	250	100	V
All Other Devices	1500	150	V

LM393, LM393E, LM293, LM2903, LM2903E, LM2903V, NCV2903

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc, $T_{low} \leq T_A \leq T_{high}$, unless otherwise noted.)

Characteristic	Symbol	LM293, LM393, LM393E			LM2903/E/V, NCV2903			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (Note 4) $T_A = 25°C$ $T_{low} \leq T_A \leq T_{high}$	V_{IO}	 – –	 ±1.0 –	 ±5.0 ±9.0	 – –	 ±2.0 ±9.0	 ±7.0 ±15	mV
Input Offset Current $T_A = 25°C$ $T_{low} \leq T_A \leq T_{high}$	I_{IO}	 – –	 ±5.0 –	 ±50 ±150	 – –	 ±5.0 ±50	 ±50 ±200	nA
Input Bias Current (Note 5) $T_A = 25°C$ $T_{low} \leq T_A \leq T_{high}$	I_{IB}	 – –	 20 –	 250 400	 – –	 20 20	 250 500	nA
Input Common Mode Voltage Range (Note 6) $T_A = 25°C$ $T_{low} \leq T_A \leq T_{high}$	V_{ICR}	 0 0	 – –	 V_{CC} –1.5 V_{CC} –2.0	 0 0	 – –	 V_{CC} –1.5 V_{CC} –2.0	V
Voltage Gain $R_L \geq 15$ kΩ, V_{CC} = 15 Vdc, $T_A = 25°C$	A_{VOL}	50	200	–	25	200	–	V/mV
Large Signal Response Time V_{in} = TTL Logic Swing, V_{ref} = 1.4 Vdc V_{RL} = 5.0 Vdc, R_L = 5.1 kΩ, $T_A = 25°C$	–	–	300	–	–	300	–	ns
Response Time (Note 7) V_{RL} = 5.0 Vdc, R_L = 5.1 kΩ, $T_A = 25°C$	t_{TLH}	–	1.3	–	–	1.5	–	μs
Input Differential Voltage (Note 8) All $V_{in} \geq$ GND or V– Supply (if used)	V_{ID}	–	–	V_{CC}	–	–	V_{CC}	V
Output Sink Current $V_{in} \geq 1.0$ Vdc, V_{in+} = 0 Vdc, $V_O \leq 1.5$ Vdc $T_A = 25°C$	I_{Sink}	6.0	16	–	6.0	16	–	mA
Output Saturation Voltage $V_{in} \geq 1.0$ Vdc, V_{in+} = 0, $I_{Sink} \leq 4.0$ mA, $T_A = 25°C$ $T_{low} \leq T_A \leq T_{high}$	V_{OL}	 – –	 150 –	 400 700	 – –	 – 200	 400 700	mV
Output Leakage Current $V_{in–}$ = 0 V, $V_{in+} \geq 1.0$ Vdc, V_O = 5.0 Vdc, $T_A = 25°C$ $V_{in–}$ = 0 V, $V_{in+} \geq 1.0$ Vdc, V_O = 30 Vdc, $T_{low} \leq T_A \leq T_{high}$	I_{OL}	 – –	 0.1 –	 – 1000	 – –	 0.1 –	 – 1000	nA
Supply Current $R_L = \infty$ Both Comparators, $T_A = 25°C$ $R_L = \infty$ Both Comparators, V_{CC} = 30 V	I_{CC}	 – –	 0.4 –	 1.0 2.5	 – –	 0.4 –	 1.0 2.5	mA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

LM293 T_{low} = −25°C, T_{high} = +85°C
LM393, LM393E T_{low} = 0°C, T_{high} = +70°C
LM2903, LM2903E T_{low} = −40°C, T_{high} = +105°C
LM2903V & NCV2903 T_{low} = −40°C, T_{high} = +125°C
NCV2903 is qualified for automotive use.

3. The maximum output current may be as high as 20 mA, independent of the magnitude of V_{CC}, output short circuits to V_{CC} can cause excessive heating and eventual destruction.
4. At output switch point, $V_O \approx 1.4$ Vdc, R_S = 0 Ω with V_{CC} from 5.0 Vdc to 30 Vdc, and over the full input common mode range (0 V to V_{CC} = −1.5 V).
5. Due to the PNP transistor inputs, bias current will flow out of the inputs. This current is essentially constant, independent of the output state, therefore, no loading changes will exist on the input lines.
6. Input common mode of either input should not be permitted to go more than 0.3 V negative of ground or minus supply. The upper limit of common mode range is V_{CC} −1.5 V.
7. Response time is specified with a 100 mV step and 5.0 mV of overdrive. With larger magnitudes of overdrive faster response times are obtainable.
8. The comparator will exhibit proper output state if one of the inputs becomes greater than V_{CC}, the other input must remain within the common mode range. The low input state must not be less than −0.3 V of ground or minus supply.
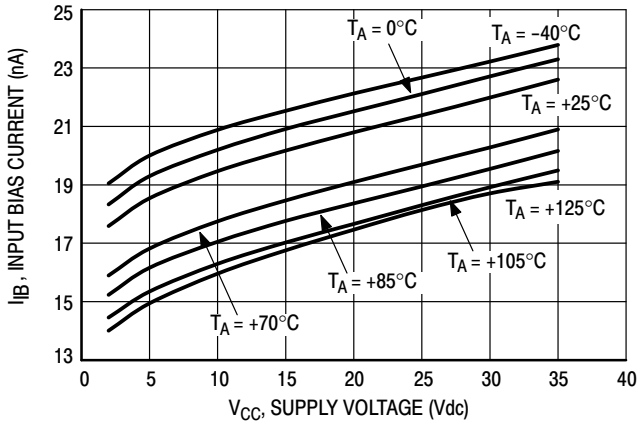
LM293/393

LM2903

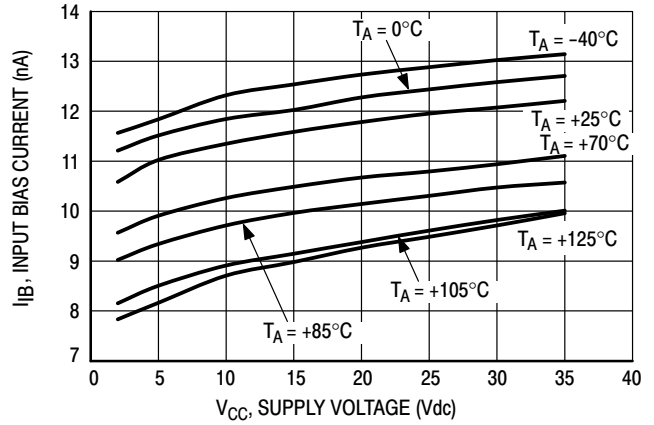Figure 2. Input Bias Current versus
Power Supply Voltage

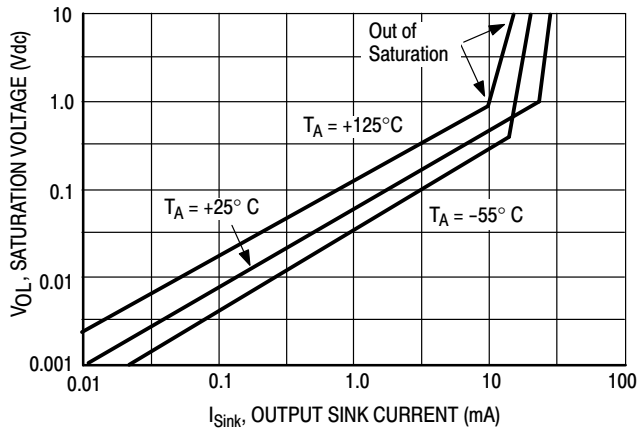Figure 3. Input Bias Current versus
Power Supply Voltage

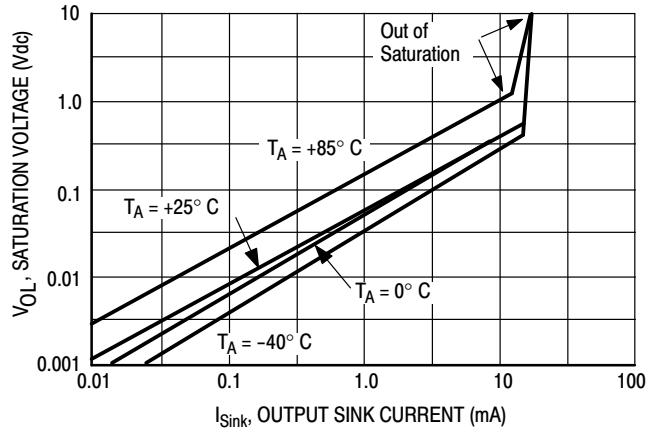Figure 4. Output Saturation Voltage
versus Output Sink Current

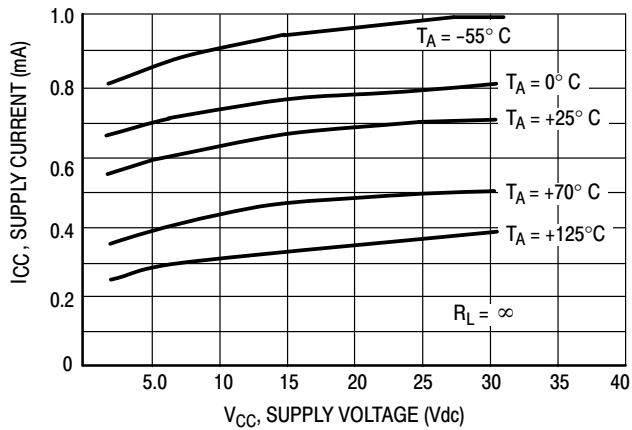Figure 5. Output Saturation Voltage
versus Output Sink Current

Figure 6. Power Supply Current versus
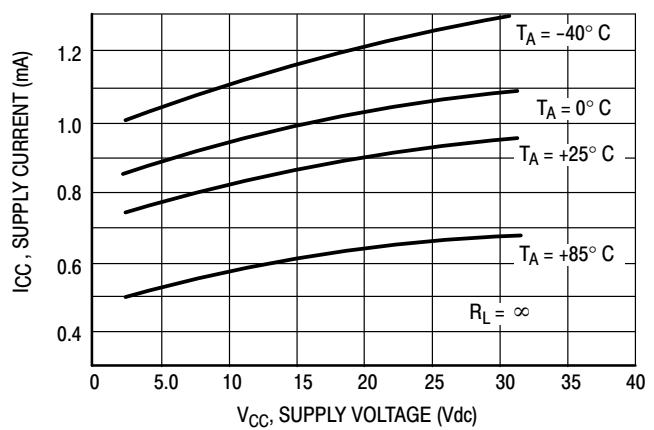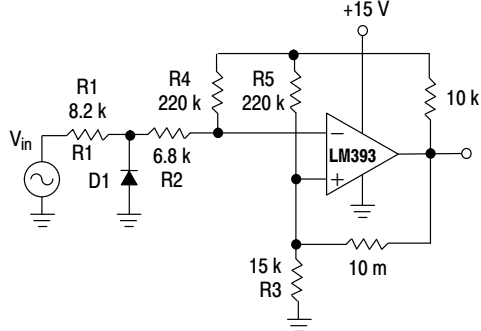Power Supply Voltage

Figure 7. Power Supply Current versus
Power Supply Voltage

LM393, LM393E, LM293, LM2903, LM2903E, LM2903V, NCV2903

APPLICATIONS INFORMATION

These dual comparators feature high gain, wide bandwidth characteristics. This gives the device oscillation tendencies if the outputs are capacitively coupled to the inputs via stray capacitance. This oscillation manifests itself during output transitions (V_{OL} to V_{OH}). To alleviate this situation, input resistors <10 kΩ should be used.

The addition of positive feedback (<10 mV) is also recommended. It is good design practice to ground all unused pins.

Differential input voltages may be larger than supply voltage without damaging the comparator's inputs. Voltages more negative than −0.3 V should not be used.

D1 prevents input from going negative by more than 0.6 V.

$$R1 + R2 = R3$$

$$R3 \leq \frac{R5}{10} \text{ for small error in zero crossing.}$$

Figure 8. Zero Crossing Detector (Single Supply)
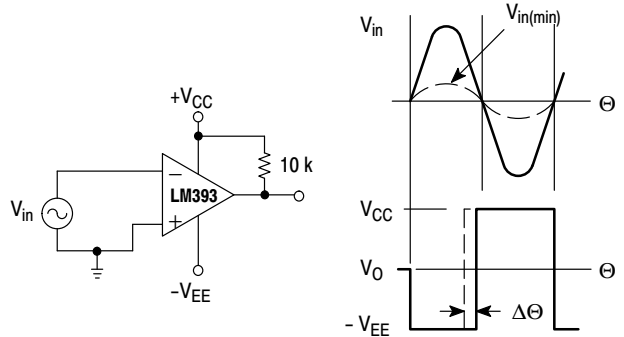
$V_{in(min)} \approx 0.4$ V peak for 1% phase distortion ($\Delta\Theta$).

Figure 9. Zero Crossing Detector (Split Supply)
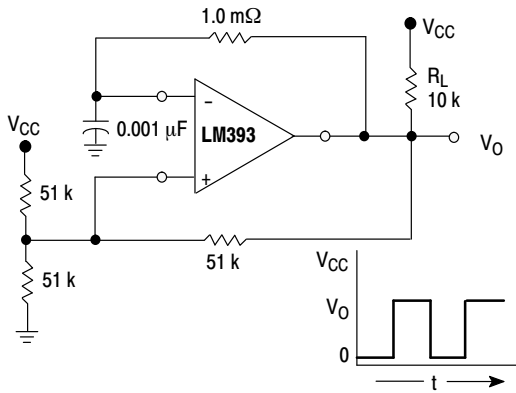
Figure 10. Free–Running Square–Wave Oscillator
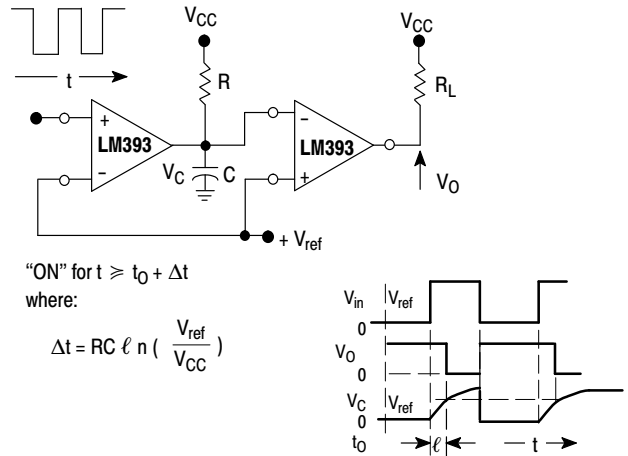
"ON" for $t \geq t_O + \Delta t$
where:

$$\Delta t = RC \ell n \left(\frac{V_{ref}}{V_{CC}} \right)$$

Figure 11. Time Delay Generator
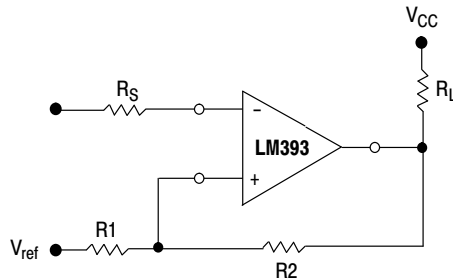
$$R_S = R1 \,|\,|\, R2$$

$$V_{th1} = V_{ref} + \frac{(V_{CC} - V_{ref})\, R1}{R1 + R2 + R_L}$$

$$V_{th2} = V_{ref} - \frac{(V_{ref} - V_O\, \text{Low})\, R1}{R1 + R2}$$
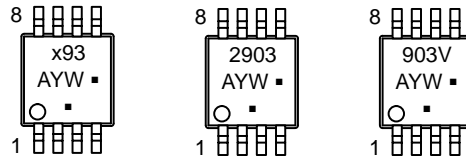
Figure 12. Comparator with Hysteresis

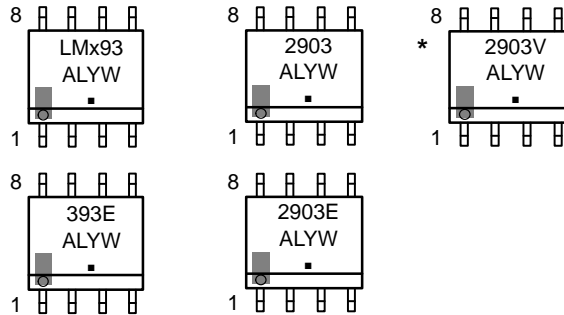# LM393, LM393E, LM293, LM2903, LM2903E, LM2903V, NCV2903

MARKING DIAGRAMS

PDIP−8
CASE 626

8

```
LM393NG
AWL
YYWW
```

1

8

```
LM2903N
AWL
YYWWG
```

1

Micro8
CASE 846A

8

```
x93
AYW ▪
```

1

8

```
2903
AYW ▪
```

1

8

```
903V
AYW ▪
```

1

SOIC−8
CASE 751

8

```
LMx93
ALYW
▪
```

1

8

```
2903
ALYW
▪
```

1

8 *

```
2903V
ALYW
▪
```

1

8

```
393E
ALYW
▪
```

1

8

```
2903E
ALYW
▪
```
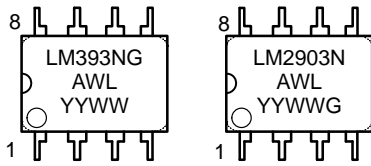
1

x	= 2 or 3
A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week
▪, G	= Pb−Free Package

(Note: Microdot may be in either location)

*This marking diagram also applies to NCV2903DR2G

https://www.vertex-icbuy.com/

ORDERING INFORMATION

Device	Operating Temperature Range	Package	Shipping†
LM293DG		SOIC−8 (Pb−Free)	98 Units / Rail
LM293DR2G	−25°C to +85°C	SOIC−8 (Pb−Free)	2500 / Tape & Reel
LM293DMR2G		Micro8 (Pb−Free)	4000 / Tape and Reel
LM393DG		SOIC−8 (Pb−Free)	98 Units / Rail
LM393DR2G		SOIC−8 (Pb−Free)	2500 / Tape & Reel
LM393EDR2G	0°C to +70°C	SOIC−8 (Pb−Free)	2500 / Tape & Reel
LM393NG		PDIP−8 (Pb−Free)	50 Units / Rail
LM393DMR2G		Micro8 (Pb−Free)	4000 / Tape and Reel
LM2903DG		SOIC−8 (Pb−Free)	98 Units / Rail
LM2903DR2G		SOIC−8 (Pb−Free)	2500 / Tape & Reel
LM2903EDR2G	−40°C to +105°C	SOIC−8 (Pb−Free)	2500 / Tape & Reel
LM2903DMR2G		Micro8 (Pb−Free)	4000 / Tape and Reel
LM2903NG		PDIP−8 (Pb−Free)	50 Units / Rail
LM2903VDG		SOIC−8 (Pb−Free)	98 Units / Rail
LM2903VDR2G		SOIC−8 (Pb−Free)	2500 / Tape & Reel
LM2903VNG	−40°C to +125°C	PDIP−8 (Pb−Free)	50 Units / Rail
NCV2903DR2G*		SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCV2903DMR2G*		Micro8 (Pb−Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

https://www.vertex-icbuy.com/

PDIP−8
CASE 626−05
ISSUE P

DATE 22 APR 2015

SCALE 1:1

TOP VIEW

NOTE 8

END VIEW
WITH LEADS CONSTRAINED
NOTE 5

SIDE VIEW

8X b

⊕ | 0.010 Ⓜ | C | A Ⓜ | B Ⓜ

END VIEW
NOTE 6
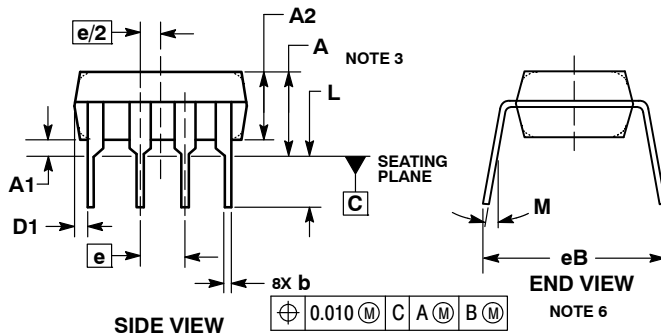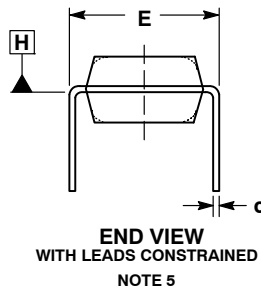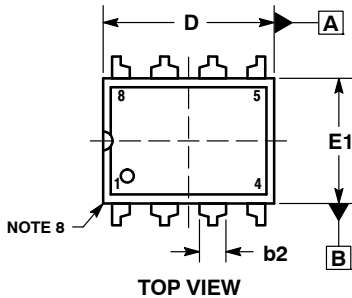
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACK-AGE SEATED IN JEDEC SEATING PLANE GAUGE GS−3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	----	0.210	---	5.33
A1	0.015	----	0.38	---
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.355	0.400	9.02	10.16
D1	0.005	----	0.13	---
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	----	0.430	---	10.92
L	0.115	0.150	2.92	3.81
M	----	10°	---	10°

STYLE 1:
PIN 1. AC IN
2. DC + IN
3. DC − IN
4. AC IN
5. GROUND
6. OUTPUT
7. AUXILIARY
8. V$_{CC}$

GENERIC
MARKING DIAGRAM*

XXXXXXXXX
AWL
YYWWG
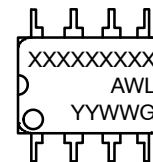
XXXX	= Specific Device Code
A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present.

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MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

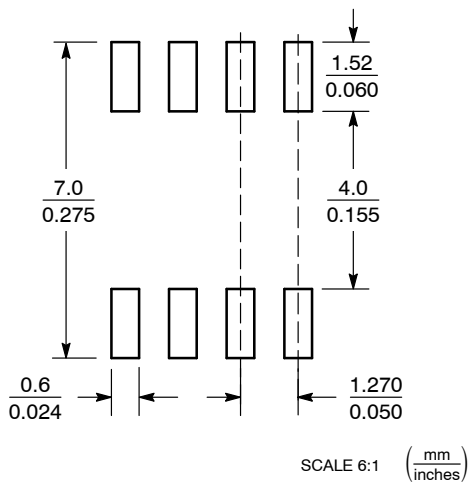**SOIC−8 NB**
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

8

1
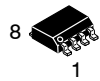
SCALE 1:1
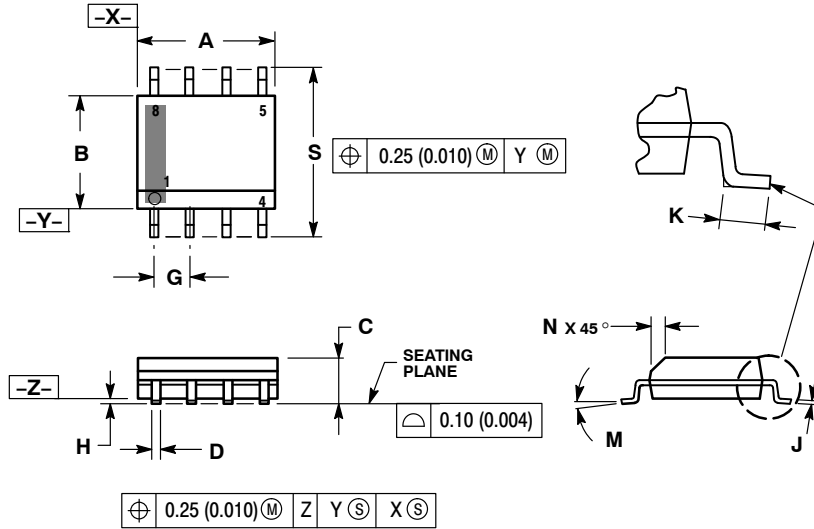
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

⊕ 0.25 (0.010) Ⓜ Y Ⓜ

⊕ 0.25 (0.010) Ⓜ Z Y Ⓢ X Ⓢ

SEATING PLANE

⌓ 0.10 (0.004)

N X 45 °

GENERIC MARKING DIAGRAM*

8   XXXXX ALYWX   1
IC

8   XXXXX ALYWX   1
IC (Pb−Free)

8   XXXXXX AYWW   1
Discrete

8   XXXXXX AYWW   1
Discrete (Pb−Free)
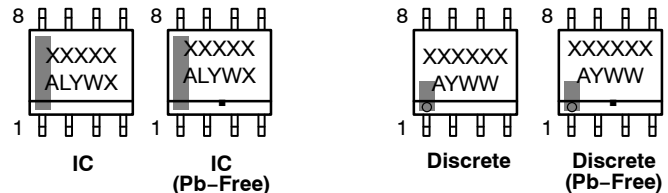
XXXXX = Specific Device Code
A   = Assembly Location
L   = Wafer Lot
Y   = Year
W   = Work Week
▪   = Pb−Free Package

XXXXXX = Specific Device Code
A   = Assembly Location
Y   = Year
WW   = Work Week
▪   = Pb−Free Package

SOLDERING FOOTPRINT*

1.52 / 0.060

7.0 / 0.275

4.0 / 0.155

0.6 / 0.024

1.270 / 0.050

SCALE 6:1 (mm / inches)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

https://www.vertex-icbuy.com/

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DESCRIPTION:	SOIC−8 NB		PAGE 1 OF 2

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
   2. COLLECTOR
   3. COLLECTOR
   4. EMITTER
   5. EMITTER
   6. BASE
   7. BASE
   8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
   2. COLLECTOR, #1
   3. COLLECTOR, #2
   4. COLLECTOR, #2
   5. BASE, #2
   6. EMITTER, #2
   7. BASE, #1
   8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
   2. DRAIN, #1
   3. DRAIN, #2
   4. DRAIN, #2
   5. GATE, #2
   6. SOURCE, #2
   7. GATE, #1
   8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
   2. ANODE
   3. ANODE
   4. ANODE
   5. ANODE
   6. ANODE
   7. ANODE
   8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
   2. DRAIN
   3. DRAIN
   4. DRAIN
   5. GATE
   6. GATE
   7. SOURCE
   8. SOURCE

STYLE 6:
PIN 1. SOURCE
   2. DRAIN
   3. DRAIN
   4. SOURCE
   5. SOURCE
   6. GATE
   7. GATE
   8. SOURCE

STYLE 7:
PIN 1. INPUT
   2. EXTERNAL BYPASS
   3. THIRD STAGE SOURCE
   4. GROUND
   5. DRAIN
   6. GATE 3
   7. SECOND STAGE Vd
   8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
   2. BASE, #1
   3. BASE, #2
   4. COLLECTOR, #2
   5. COLLECTOR, #2
   6. EMITTER, #2
   7. EMITTER, #1
   8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
   2. COLLECTOR, DIE #1
   3. COLLECTOR, DIE #2
   4. EMITTER, COMMON
   5. EMITTER, COMMON
   6. BASE, DIE #2
   7. BASE, DIE #1
   8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
   2. BIAS 1
   3. OUTPUT
   4. GROUND
   5. GROUND
   6. BIAS 2
   7. INPUT
   8. GROUND

STYLE 11:
PIN 1. SOURCE 1
   2. GATE 1
   3. SOURCE 2
   4. GATE 2
   5. DRAIN 2
   6. DRAIN 2
   7. DRAIN 1
   8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
   2. SOURCE
   3. SOURCE
   4. GATE
   5. DRAIN
   6. DRAIN
   7. DRAIN
   8. DRAIN

STYLE 13:
PIN 1. N.C.
   2. SOURCE
   3. SOURCE
   4. GATE
   5. DRAIN
   6. DRAIN
   7. DRAIN
   8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
   2. N−GATE
   3. P−SOURCE
   4. P−GATE
   5. P−DRAIN
   6. P−DRAIN
   7. N−DRAIN
   8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
   2. ANODE 1
   3. ANODE 1
   4. ANODE 1
   5. CATHODE, COMMON
   6. CATHODE, COMMON
   7. CATHODE, COMMON
   8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
   2. BASE, DIE #1
   3. EMITTER, DIE #2
   4. BASE, DIE #2
   5. COLLECTOR, DIE #2
   6. COLLECTOR, DIE #2
   7. COLLECTOR, DIE #1
   8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
   2. V2OUT
   3. V1OUT
   4. TXE
   5. RXE
   6. VEE
   7. GND
   8. ACC

STYLE 18:
PIN 1. ANODE
   2. ANODE
   3. SOURCE
   4. GATE
   5. DRAIN
   6. DRAIN
   7. CATHODE
   8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
   2. GATE 1
   3. SOURCE 2
   4. GATE 2
   5. DRAIN 2
   6. MIRROR 2
   7. DRAIN 1
   8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
   2. GATE (N)
   3. SOURCE (P)
   4. GATE (P)
   5. DRAIN
   6. DRAIN
   7. DRAIN
   8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
   2. CATHODE 2
   3. CATHODE 3
   4. CATHODE 4
   5. CATHODE 5
   6. COMMON ANODE
   7. COMMON ANODE
   8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
   2. COMMON CATHODE/VCC
   3. COMMON CATHODE/VCC
   4. I/O LINE 3
   5. COMMON ANODE/GND
   6. I/O LINE 4
   7. I/O LINE 5
   8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
   2. COMMON ANODE/GND
   3. COMMON ANODE/GND
   4. LINE 2 IN
   5. LINE 2 OUT
   6. COMMON ANODE/GND
   7. COMMON ANODE/GND
   8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
   2. EMITTER
   3. COLLECTOR/ANODE
   4. COLLECTOR/ANODE
   5. CATHODE
   6. CATHODE
   7. COLLECTOR/ANODE
   8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
   2. N/C
   3. REXT
   4. GND
   5. IOUT
   6. IOUT
   7. IOUT
   8. IOUT

STYLE 26:
PIN 1. GND
   2. dv/dt
   3. ENABLE
   4. ILIMIT
   5. SOURCE
   6. SOURCE
   7. SOURCE
   8. VCC

STYLE 27:
PIN 1. ILIMIT
   2. OVLO
   3. UVLO
   4. INPUT+
   5. SOURCE
   6. SOURCE
   7. SOURCE
   8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
   2. DASIC_OFF
   3. DASIC_SW_DET
   4. GND
   5. V_MON
   6. VBULK
   7. VBULK
   8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
   2. EMITTER, #1
   3. BASE, #2
   4. EMITTER, #2
   5. COLLECTOR, #2
   6. COLLECTOR, #2
   7. COLLECTOR, #1
   8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
   2. DRAIN 1
   3. GATE 2
   4. SOURCE 2
   5. SOURCE 1/DRAIN 2
   6. SOURCE 1/DRAIN 2
   7. SOURCE 1/DRAIN 2
   8. GATE 1

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DESCRIPTION:	SOIC−8 NB		PAGE 2 OF 2

ON Semiconductor®

Micro8
CASE 846A−02
ISSUE K

SCALE 2:1

DATE 16 JUL 2020

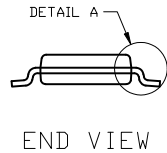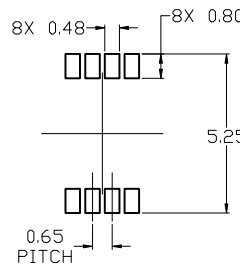**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.

2. CONTROLLING DIMENSION: MILLIMETERS

3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.

4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. DIMENSION E DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM F.

5. DATUMS A AND B ARE TO BE DETERMINED AT DATUM F.

6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

TOP VIEW

NOTE 3

$\boxed{\oplus \; 0.08 \; (0.003) \; \text{M} \; \text{C} \; \text{B} \; \text{S} \; \text{A} \; \text{S}}$

8X b

DETAIL A

SIDE VIEW

$\boxed{\triangle \; 0.038 \; (0.0015) \; C}$

END VIEW

DETAIL A

8X 0.48 — 8X 0.80

5.25

0.65 PITCH

RECOMMENDED MOUNTING FOOTPRINT

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	1.10
A1	0.05	0.08	0.15
b	0.25	0.33	0.40
c	0.13	0.18	0.23
D	2.90	3.00	3.10
E	2.90	3.00	3.10
e	0.65 BSC		
H_E	4.75	4.90	5.05
L	0.40	0.55	0.70

■ For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*

8

XXXX
AYW■

1
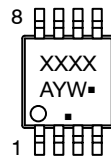
XXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
■ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 2:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 3:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

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