DC to 50 MHz, Dual I/Q Demodulator and Phase Shifter

Data Sheet **AD8333**

FEATURES

Dual integrated I/Q demodulator
16 phase select options on each output (22.5° per step)
Quadrature demodulation accuracy
- **Phase accuracy: ±0.1°**
- **Amplitude balance: ±0.05 dB**

Bandwidth
- **4 × LO: 10 kHz to 200 MHz**
- **RF: dc to 50 MHz**
- **Baseband: determined by external filtering**

Output dynamic range: 159 dB/Hz
LO drive > 0 dBm (50 Ω); 4 × LO > 1 MHz
Supply: ±5 V
Power consumption: 190 mW/channel (380 mW total)
Power-down

APPLICATIONS

Medical imaging (CW ultrasound beamforming)
Phased array systems (radar and adaptive antennas)
Communication receivers

FUNCTIONAL BLOCK DIAGRAM

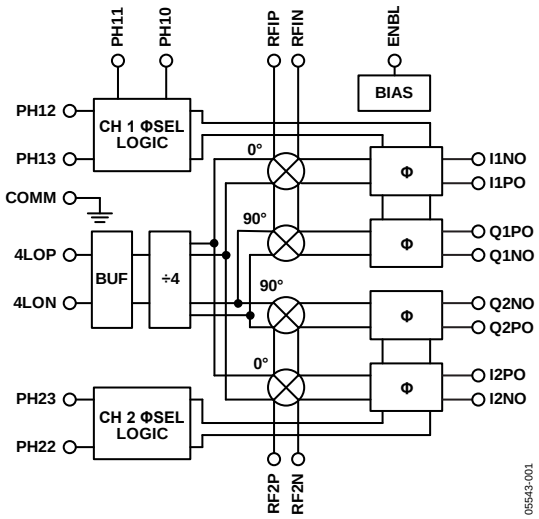

Figure 1.

GENERAL DESCRIPTION

The AD8333[1] is a dual phase-shifter and I/Q demodulator that enables coherent summing and phase alignment of multiple analog data channels. It is the first solid-state device suitable for beamformer circuits, such as those used in high performance medical ultrasound equipment featuring CW Doppler. The RF inputs interface directly with the outputs of the dual-channel, low noise preamplifiers included in the AD8332.

A divide-by-4 circuit generates the internal 0° and 90° phases of the local oscillator (LO) that drive the mixers of a pair of matched I/Q demodulators.

The AD8333 can be applied as a major element in analog beamformer circuits in medical ultrasound equipment.

The AD8333 features an asynchronous reset pin. When used in arrays, the reset pin sets all the LO dividers in the same state. Sixteen discrete phase rotations in 22.5° increments can be selected independently for each channel. For example, if Channel 1 is used as a reference and the RF signal applied to Channel 2 has an I/Q phase lead of 45°, Channel 2 can be phase aligned with Channel 1 by choosing the correct code.

Phase shift is defined by the output of one channel relative to another. For example, if the code of Channel 1 is adjusted to 0000 and that of Channel 2 is adjusted to 0001 and the same signal is applied to both RF inputs, the output of Channel 2 leads that of Channel 1 by 22.5°.

The I and Q outputs are provided as currents to facilitate summation. The summed current outputs are converted to voltages by a high dynamic range, current-to-voltage (I-V) converter, such as the AD8021, configured as a transimpedance amplifier. The resultant signal is then applied to a high resolution ADC, such as the AD7665 (16 bit/570 kSPS).

The two I/Q demodulators can be used independently in other nonbeamforming applications. In that case, a transimpedance amplifier is needed for each of the I and Q outputs, four in total for the dual I/Q demodulator.

The dynamic range is 159 dB/Hz at the I and Q outputs, but the following transimpedance amplifier is an important element in maintaining the overall dynamic range, and attention needs to be paid to optimal component selection and design.

The AD8333 is available in a 32-lead LFCSP (5 mm × 5 mm) package for the industrial temperature range of −40°C to +85°C.

[1] Protected by US Patent 7,760,833.

Rev. F **Document Feedback**

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TABLE OF CONTENTS

REVISION HISTORY

5/2016—Rev. E to Rev. F

Change to Features Section and General Description Section.....1
Change to Quiescent Power Parameter, Table 1.....5
Changes to Figure 2 and Table 3 7
Change to Figure 52 18
Change to Figure 61 28
Change to Figure 64 29
Updated Outline Dimensions.....32
Changes to Ordering Guide.....32

8/2012—Rev. D to Rev. E

Changes to Figure 1 and General Description Section 1
Moved Revision History Section.....3
Changes to Table 3 7
Changes to Table 5 27
Updated Outline Dimensions.....33

9/2010—Rev. C to Rev. D

Change to I2NO, Q2NO, Q1NO, and I1NO Pin Description, Table 3 6
Changes to Figure 62, Features and Options Section, Table 5, Phase Nibble Section, and Enable and Reset Switches Section 26
Changes to Reset Input Section, Measurement Setup Section, and Figure 63 27
Changes to Figure 64 28
Changes to Figure 65 29
Changes to Figure 66 Through Figure 70 30
Deleted Ordering Information Section 37
Deleted Table 7; Renumbered Sequentially 37

9/2008—Rev. B to Rev. C

Changes to Figure 1.....1
Changes to General Description Section 1
Change to Table 2 5
Changes to Figure 4 and Figure 6.....7
Change to Figure 18 9
Changes to Dynamic Range and Noise Section 18
Changes to Connecting to the LNA of the AD8331/AD8332/AD8334/AD8335 VGAs Section 24
Added Interfacing to Other Amplifiers Heading.....25
Changes to Figure 61 25
Incorporated AD8333-EVALZ Data Sheet 26
Changes to Evaluation Board Section 26
Changes to Features and Options Section 26
Changes to Table 5 26
Replaced the Phase Bits Section with the Phase Nibble Section 26
Deleted Table 2 3
Changes to LNA Input Impedance Section 26
Changes to Current Summing Section.....26
Changes to Measurement Setup Section.....27
Moved Figure 63; Changes to Figure 63.....27
Changes to Figure 64 28
Moved Figure 70.....30
Changes to Table 7 31
Deleted Figure 62; Renumbered Sequentially 26
Updated Outline Dimensions.....32
Changes to Ordering Guide.....32

5/2007—Rev. A to Rev. B

Changes to Features and Figure 1 1
Changes to Table 1 3
Changes to Figure 41 to Figure 43 14
Changes to Figure 44 to Figure 47 15
Changes to Figure 48 to Figure 51 16
Changes to Figure 55 20
Changes to Evaluation Board Section 25
Changes to Ordering Guide.....27

5/2006—Rev. 0 to Rev. A

Changes to Figure 62 26

10/2005—Revision 0: Initial Version

SPECIFICATIONS

V_S = ±5 V, T_A = 25°C, f_{4LO} = 20 MHz, f_{RF} = 5.01 MHz, f_{BB} = 10 kHz, P_{LO} ≥ 0 dBm, single-ended, sine wave; per channel performance, dBm (50 Ω), unless otherwise noted (see Figure 41).

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
OPERATING CONDITIONS					
LO Frequency Range	4× internal LO at Pin 4LOP and Pin 4LON				
	Square wave	0.01		200	MHz
	Sine wave, see Figure 22	2		200	MHz
RF Frequency Range	Mixing	DC		50	MHz
Baseband Bandwidth	Limited by external filtering	DC		50	MHz
LO Input Level	See Figure 22		0	13	dBm
V_{SUPPLY} (V_S)		±4.5	±5	±6	V
Temperature Range		−40		+85	°C
DEMODULATOR PERFORMANCE					
RF Differential Input Impedance			6.7||6.5		kΩ||pF
LO Differential Input Capacitance			0.6		pF
Transconductance	Demodulated I_{OUT}/V_{IN}, each I or Q output after low-pass filtering measured from RF inputs, all phases		2.17		mS
Dynamic Range	IP1dB, input-referred noise (dBm)		159		dB/Hz
Maximum RF Input Swing	Differential; inputs biased at 2.5 V; Pin RFxP and Pin RFxN		2.8		V p-p
Peak Output Current (No Filtering)	0° phase shift		±4.7		mA
	45° phase shift		±6.6		mA
Input P1dB	Reference = 50 Ω		14.5		dBm
	Reference = 1 V rms		1.5		dBV
Third-Order Intermodulation (IM3)	f_{RF1} = 5.010 MHz, f_{RF2} = 5.015 MHz, f_{LO} = 5.023 MHz				
Equal Input Levels	Baseband tones: −7 dBm at 8 kHz and 13 kHz		−75		dBc
Unequal Input Levels	Baseband tones: −1 dBm at 8 kHz and −31 dBm at 13 kHz		−77		dBc
Third-Order Input Intercept (IP3)	f_{RF1} = 5.010 MHz, f_{RF2} = 5.015 MHz, f_{LO} = 5.023 MHz		30		dBm
LO Leakage	Measured at RF inputs, worst phase, measured into 50 Ω (limited by measurement)		<−97		dBm
	Measured at baseband outputs, worst phase, AD8021 disabled, measured into 50 Ω		−60		dBm
Conversion Gain	All codes		4.7		dB
Input-Referred Noise	Output noise/conversion gain		10		nV/√Hz
Output Current Noise	Output noise ÷ 787 Ω		22		pA/√Hz
Noise Figure	With AD8332 LNA				
	R_S = 50 Ω, R_{FB} = ∞		7.8		dB
	R_S = 50 Ω, R_{FB} = 1.1 kΩ		9.0		dB
	R_S = 50 Ω, R_{FB} = 274 Ω		11.0		dB
Bias Current	Pin 4LOP and Pin 4LON		−3		µA
	Pin RFxP and Pin RFxN		−70		µA
LO Common-Mode Voltage Range	Pin 4LOP and Pin 4LON (each pin)	0.2		3.8	V
RF Common-Mode Voltage	For maximum differential swing; Pin RFxP and Pin RFxN (dc-coupled to AD8332 LNA output)		2.5		V
Output Compliance Range	Pin IxPO and Pin QxPO	−1.5		+0.7	V
PHASE ROTATION PERFORMANCE	One channel is reference; the other channel is stepped				
Phase Increment	16 phase steps per channel		22.5		Degrees
Quadrature Phase Error	I1xO to Q1xO and I2xO to Q2xO, 1σ	−2	±0.1	+2	Degrees
I/Q Amplitude Imbalance	I1xO to Q1xO and I2xO to Q2xO, 1σ		±0.05		dB
Channel-to-Channel Matching	Phase match I1xO/I2xO and Q1xO/Q2xO; −40°C < T_A < 85°C		±1		Degrees
	Amplitude match I1xO/I2xO and Q1xO/Q2xO; −40°C < T_A < 85°C		±0.25		dB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
LOGIC INTERFACES					
Logic Level High	Pin PHxx, Pin RSET, and Pin ENBL	1.7		5	V
Logic Level Low	Pin PHxx, Pin RSET, and Pin ENBL	0		1.3	V
Bias Current					
Pin PHxx and Pin ENBL	Logic high	10	40	90	µA
	Logic low	−30	−7	+10	µA
Pin RSET	Logic high	50	120	180	µA
	Logic low	−70	−20	0	µA
Input Resistance	Pin PHxx and Pin ENBL		60		kΩ
	Pin RSET		20		kΩ
Reset Hold Time	Reset is asynchronous; clock disabled when RSET goes high until 300 ns after RSET goes low; see Figure 58	300			ns
Minimum Reset Pulse Width		300			ns
Reset Response Time	See Figure 35		300		ns
Phase Shifting Response Time	See Figure 38		5		µs
Enable Response Time	See Figure 34		300		ns
POWER SUPPLY	Pin VPOS and Pin VNEG				
Supply Voltage		±4.5	±5	±6	V
Quiescent Current, All Phase Bits = 0	At 25°C				
	Pin VPOS	38	44	51	mA
	Pin VNEG	−24	−20	−16	mA
Over Temperature	$-40°C < T_A < 85°C$				
	Pin VPOS, all phase bits = 0	40		54	mA
	Pin VNEG	−24		−19	mA
Quiescent Power	Per channel, all phase bits = 0		160		mW
	Per channel, any 0 or 1 combination of phase bits		190		mW
Disable Current	All channels disabled				
	Pin VPOS	1.0	1.25	1.5	mA
	Pin VNEG	−300	−200	−100	µA
PSRR					
	Pin VPOS to I/Q outputs (measured at AD8021 output)		−81		dB
	Pin VNEG to I/Q outputs (measured at AD8021 output)		−75		dB

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Voltages	
Supply Voltage, V_S	6 V
RF Pins Input	V_S, GND
LO Inputs	V_S, GND
Code Select Inputs Voltage	V_S, GND
Thermal Data[1]	
θ_{JA}	41.0°C/W
θ_{JB}	23.6°C/W
θ_{JC}	4.4°C/W
Ψ_{JT}	0.4°C/W
Ψ_{JB}	22.4°C/W
Maximum Junction Temperature	150°C
Maximum Power Dissipation (Exposed Pad Soldered to PC Board)	1.5 W
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

[1] 4-layer JEDEC board no airflow (exposed pad soldered to PCB).

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

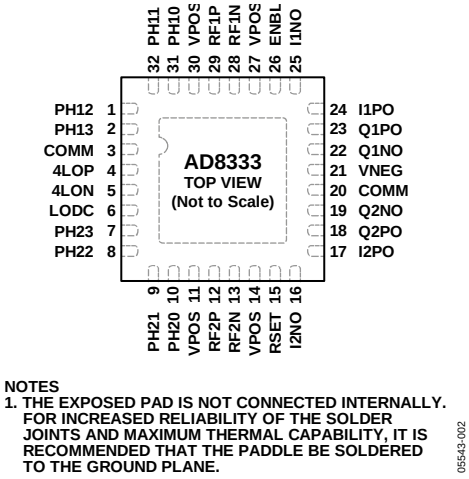


Figure 2. 32-Lead LFCSP Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 7, 8	PH12, PH13, PH23, PH22	Quadrant Select LSB, MSB. Binary code. These logic inputs select the quadrant: 0° to 90°, 90° to 180°, 180° to 270°, 270° to 360° (see Table 4). Logic threshold is at about 1.5 V and therefore can be driven by 3 V CMOS logic (see Figure 3).
3, 20	COMM	Ground. These two pins are internally tied together.
4, 5	4LOP, 4LON	LO Inputs. No internal bias; therefore, these pins need to be biased by external circuitry. For optimum performance, these inputs must be driven differentially with a signal level that is not less than what is shown in Figure 22. Bias current is only −3 µA. Single-ended drive is also possible if the inputs are biased correctly (see Figure 4).
6	LODC	Decoupling Pin for LO. A 0.1 µF capacitor must be connected between this pin and ground (see Figure 5).
9, 10, 31, 32	PH21, PH20, PH10, PH11	Phase Select LSB, MSB. Binary code. These logic inputs select the phase for a given quadrant: 0°, 22.5°, 45°, 67.5° (see Table 4). Logic threshold is at about 1.5 V and therefore can be driven by 3 V CMOS logic (see Figure 3).
11, 14, 27, 30	VPOS	Positive Supply. These pins must be decoupled with a ferrite bead in series with the supply, plus a 0.1 µF and 100 pF capacitor between the VPOS pins and ground. Because the VPOS pins are internally connected, one set of supply decoupling components for all four pins must be sufficient.
12, 13, 28, 29	RF2P, RF2N, RF1N, RF1P	RF Inputs. These pins are biased internally; however, it is recommended that they be biased by dc coupling to the output pins of the AD8332 LNA. The optimum common-mode voltage for maximum symmetrical input differential swing is 2.5 V if ±5 V supplies are used (see Figure 6 and Figure 60).
15	RSET	Reset for Divide-by-4 in LO Interface. Logic threshold is at about 1.5 V and therefore can be driven by 3 V CMOS logic (see Figure 3). Reset when high, enable when low.
16, 19, 22, 25	I2NO, Q2NO, Q1NO, I1NO	Negative I/Q Outputs. Not connected for typical applications.
17, 18, 23, 24	I2PO, Q2PO, Q1PO, I1PO	Positive I/Q Outputs. These outputs provide a bidirectional current that can be converted back to a voltage via a transimpedance amplifier. Multiple outputs can be summed together by connecting them together. The bias voltage must be set to 0 V or less by the transimpedance amplifier (see Figure 7).
21	VNEG	Negative Supply. This pin must be decoupled with a ferrite bead in series with the supply, plus a 0.1 µF and 100 pF capacitor between the pin and ground.
26	ENBL	Chip Enable. Logic threshold is at about 1.5 V and therefore can be driven by 3 V CMOS logic (see Figure 3).
	EPAD	Exposed Pad. The exposed pad is not connected internally. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the paddle be soldered to the ground plane.

EQUIVALENT INPUT CIRCUITS

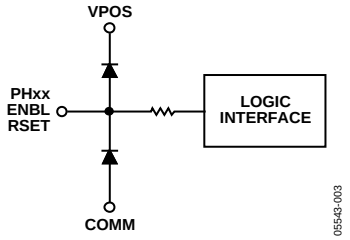


Figure 3. Logic Inputs

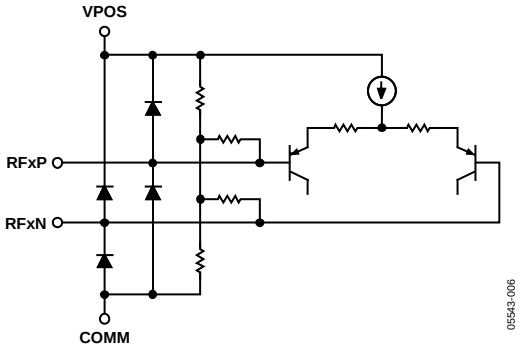


Figure 6. RF Inputs

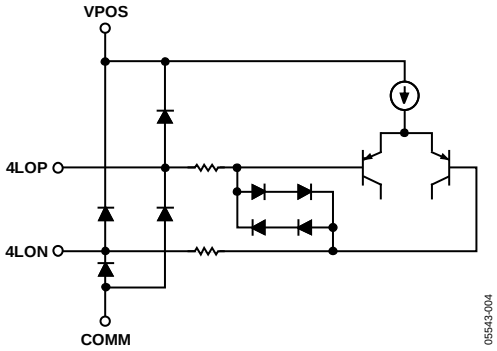


Figure 4. Local Oscillator Inputs

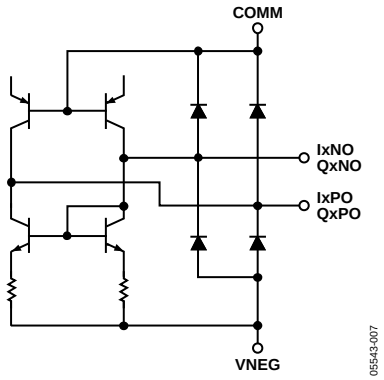


Figure 7. Output Drivers

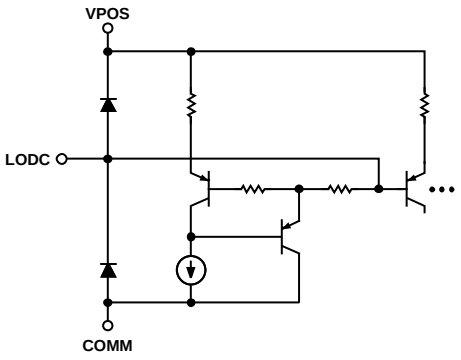


Figure 5. Local Oscillator Decoupling Pin

TYPICAL PERFORMANCE CHARACTERISTICS

V_S = ±5 V, T_A = 25°C, f_{4LO} = 20 MHz, f_{LO} = 5 MHz, f_{RF} = 5.01 MHz, f_{BB} = 10 kHz, P_{LO} ≥ 0 dBm (50 Ω); single-ended sine wave; per channel performance, differential voltages, dBm (50 Ω), phase select code = 0000, unless otherwise noted (see Figure 41).

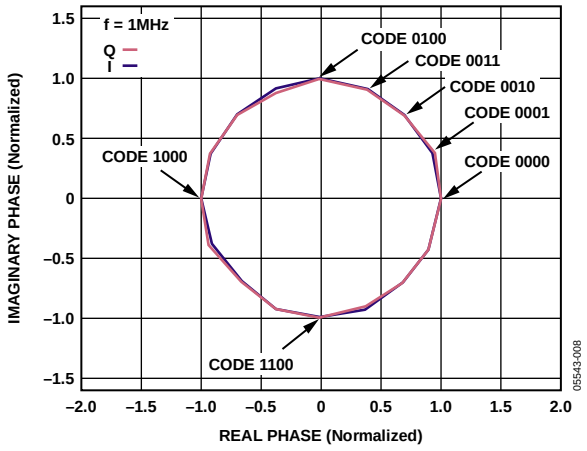


Figure 8. Normalized Vector Plot of Phase, Channel 2 with Respect to Channel 1; Channel 1 Is Fixed at 0°, Channel 2 Stepped 22.5°/Step, All Codes Displayed

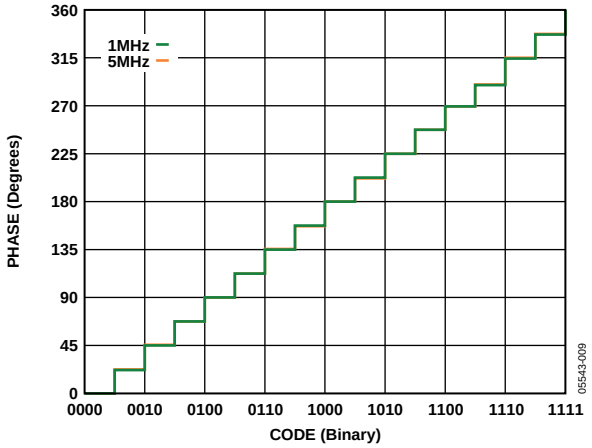


Figure 9. Phase of Channel 2 with Respect to Channel 1 vs. Code at 1 MHz and 5 MHz

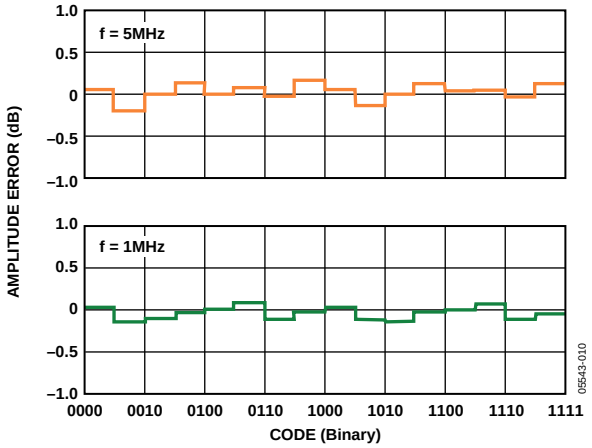


Figure 10. Amplitude Error of Channel 2 with Respect to Channel 1 vs. Code at 1 MHz and 5 MHz

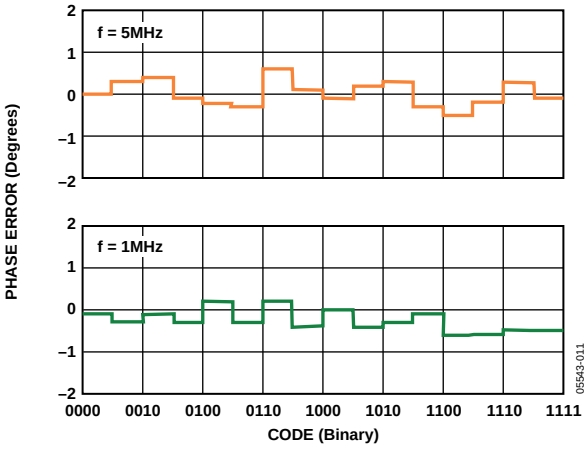


Figure 11. Phase Error of Channel 2 with Respect to Channel 1 vs. Code at 1 MHz and 5 MHz

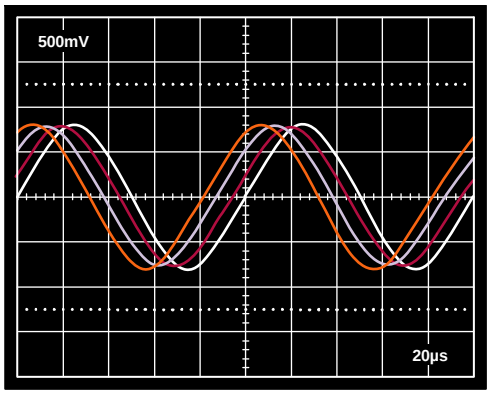


Figure 12. I or Q Output of Channel 2 with Respect to Channel 1, First Quadrant Shown

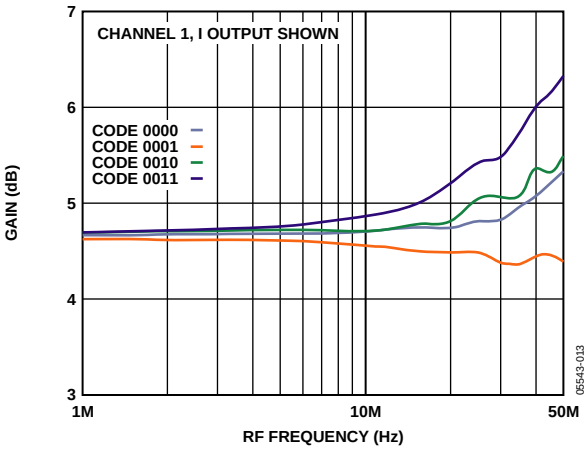


Figure 13. Conversion Gain vs. RF Frequency, First Quadrant, Baseband Frequency = 10 kHz

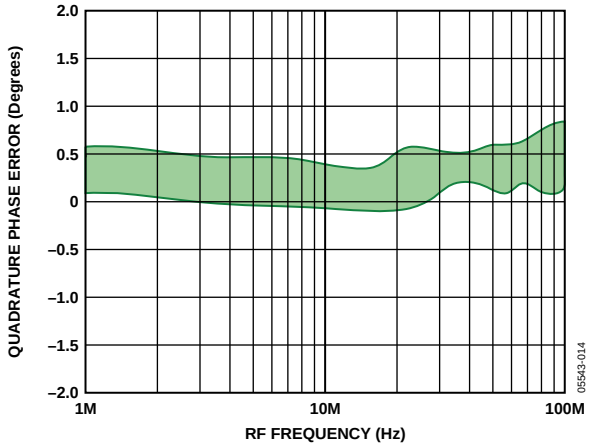


Figure 14. Representative Range of Quadrature Phase Errors vs. RF Frequency, Channel 1 or Channel 2, All Codes

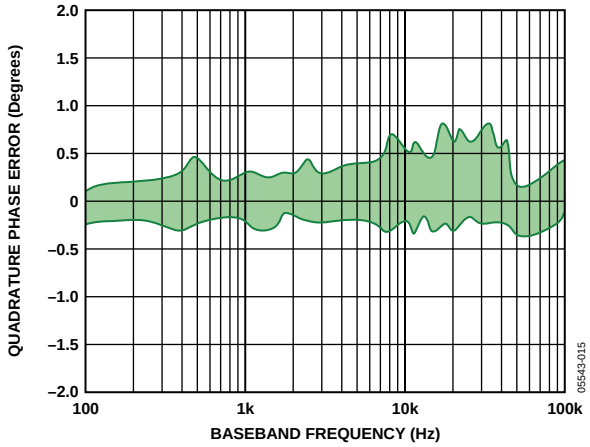


Figure 15. Representative Range of Quadrature Phase Error vs. Baseband Frequency, Channel 1 and Channel 2 (see Figure 43)

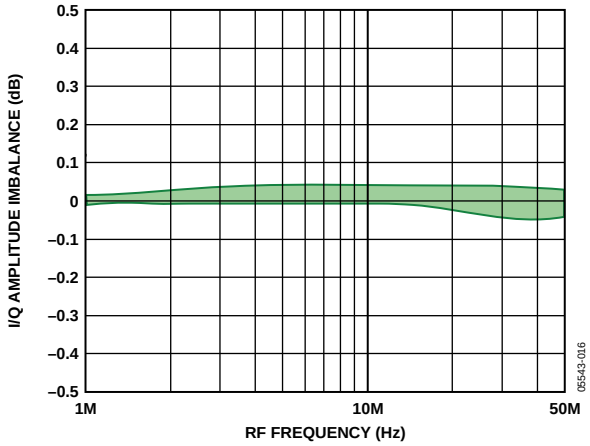


Figure 16. Representative Range of I/Q Amplitude Imbalance vs. RF Frequency, Channel 1 or Channel 2, All Codes

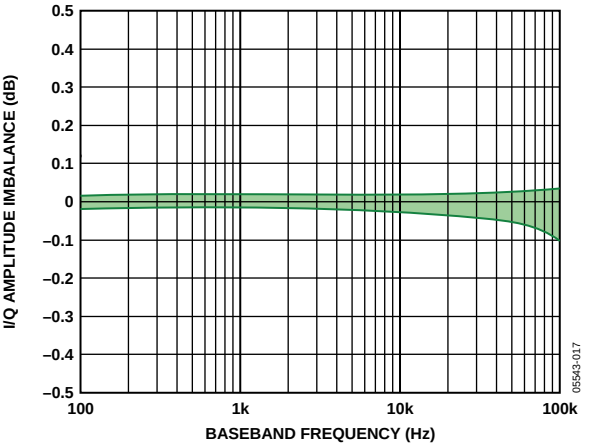


Figure 17. Representative Range of I/Q Amplitude Imbalance vs. Baseband Frequency, Channel 1 and Channel 2 (see Figure 43)

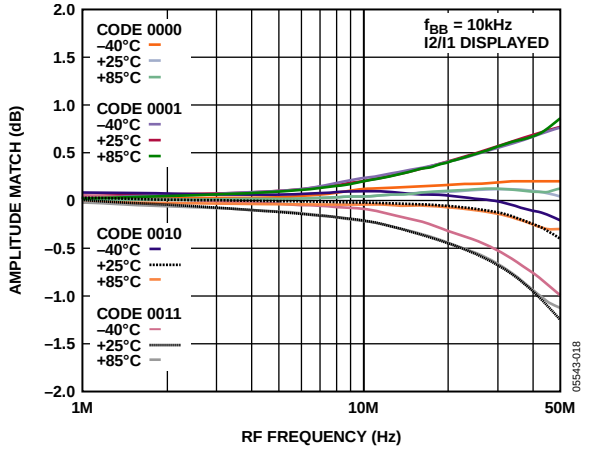


Figure 18. Typical I2xO/I1xO or Q2xO/Q1xO Amplitude Match vs. RF Frequency, First Quadrant, at Three Temperatures

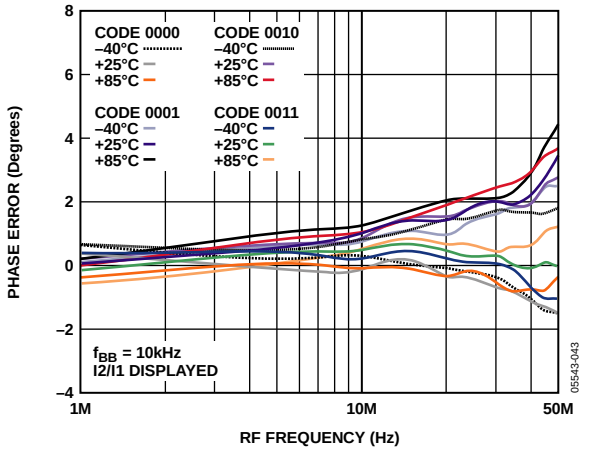


Figure 19. I2xO/I1xO or Q2xO/Q1xO Phase Error vs. RF Frequency, Baseband Frequency = 10 kHz, at Three Temperatures

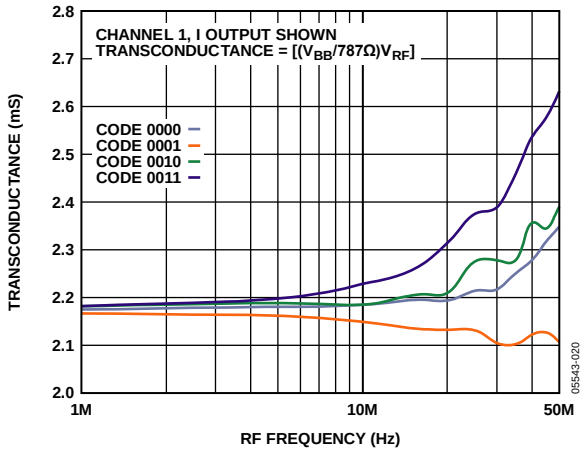


Figure 20. Transconductance vs. RF Frequency, First Quadrant

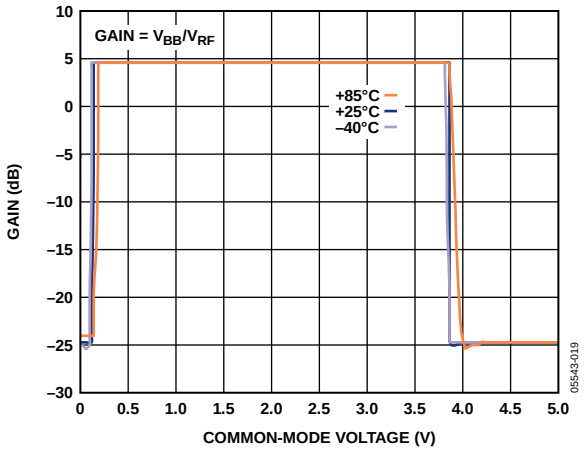


Figure 23. LO Common-Mode Range at Three Temperatures

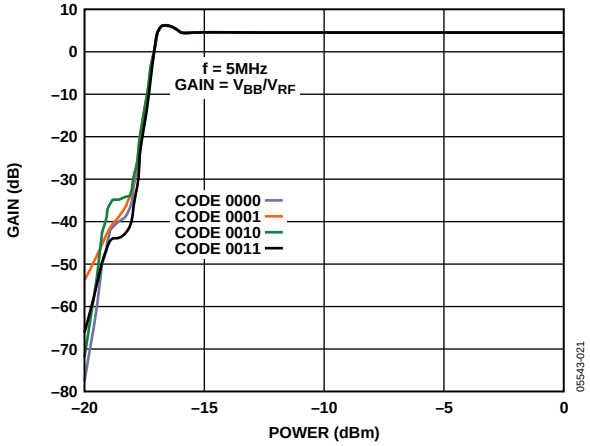


Figure 21. Conversion Gain vs. LO Level, First Quadrant

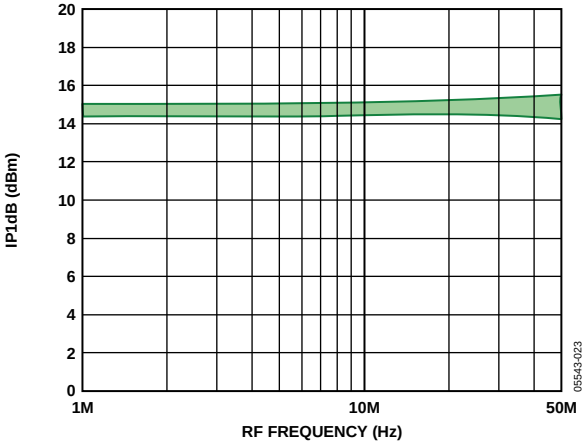


Figure 24. IP1dB vs. RF Frequency, Baseband Frequency = 10 kHz, First Quadrant (see Figure 42)

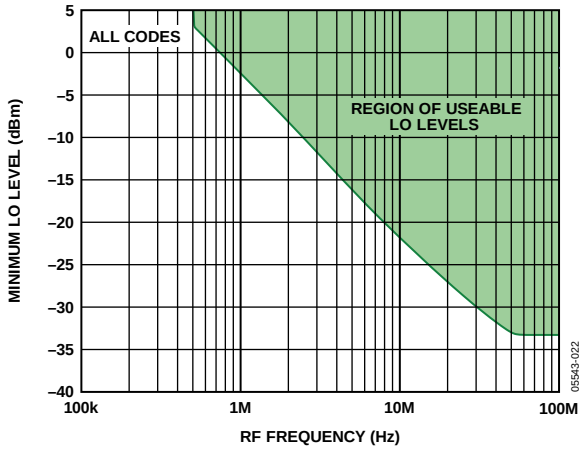


Figure 22. Minimum LO Level vs. RF Frequency, Single-Ended, Sine Wave LO Drive to Pin 4LOP or Pin 4LON

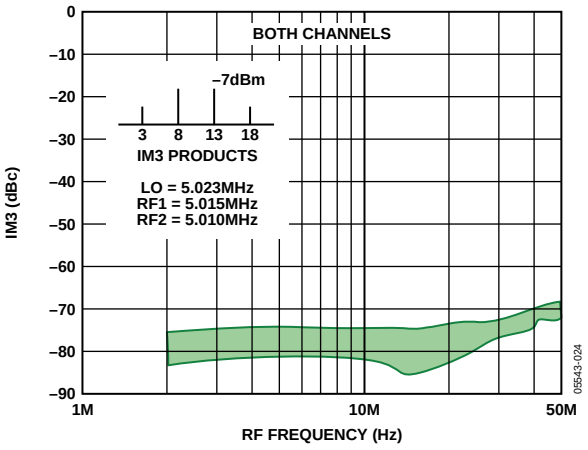


Figure 25. Representative Range of IM3 vs. RF Frequency, First Quadrant (see Figure 49)

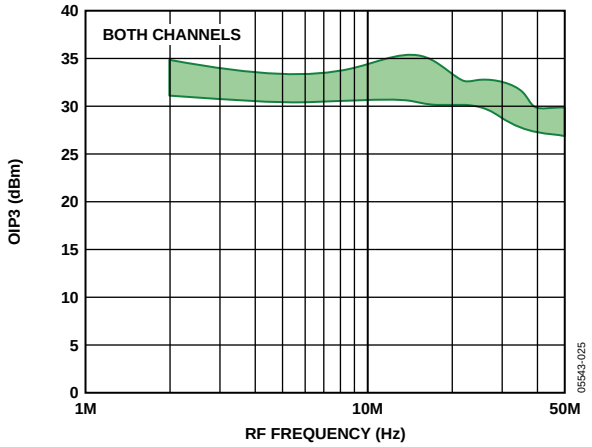


Figure 26. Representative Range of OIP3 vs. RF Frequency, First Quadrant (see Figure 49)

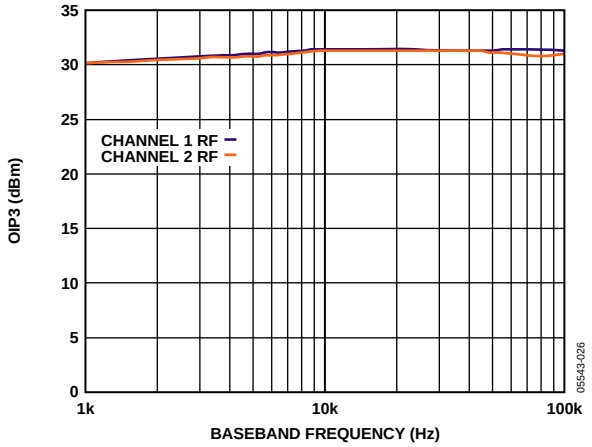


Figure 27. OIP3 vs. Baseband Frequency (see Figure 48)

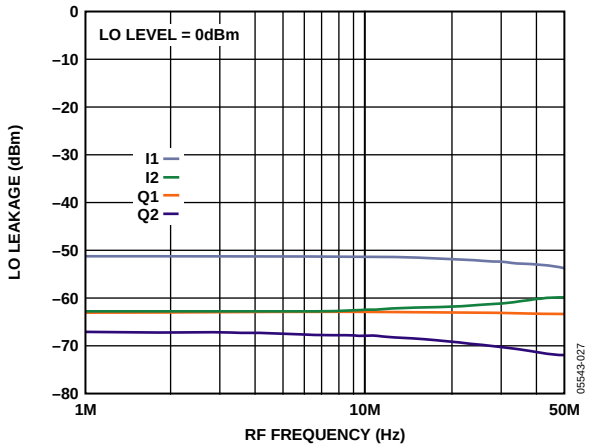


Figure 28. LO Leakage vs. RF Frequency at Baseband Outputs

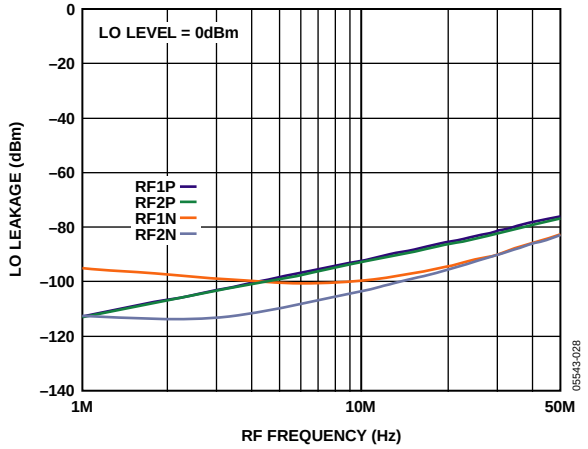


Figure 29. LO Leakage vs. RF Frequency at RF Inputs

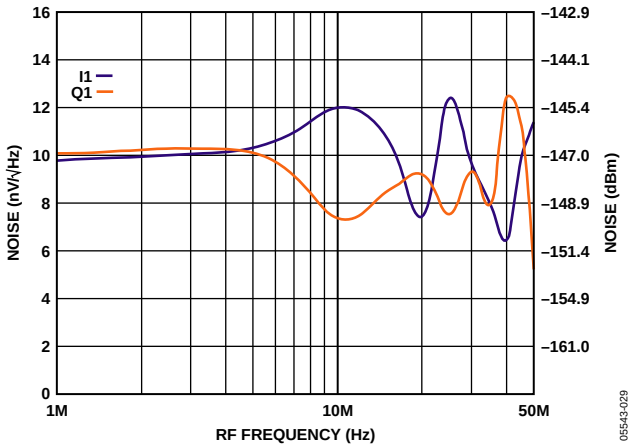


Figure 30. Input-Referred Noise vs. RF Frequency

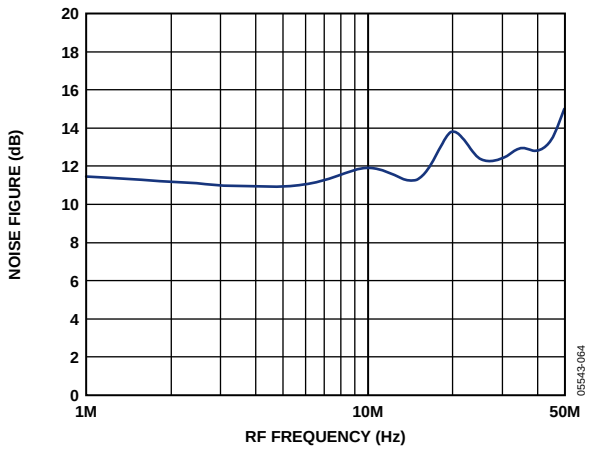


Figure 31. Noise Figure vs. RF Frequency with AD8332 LNA

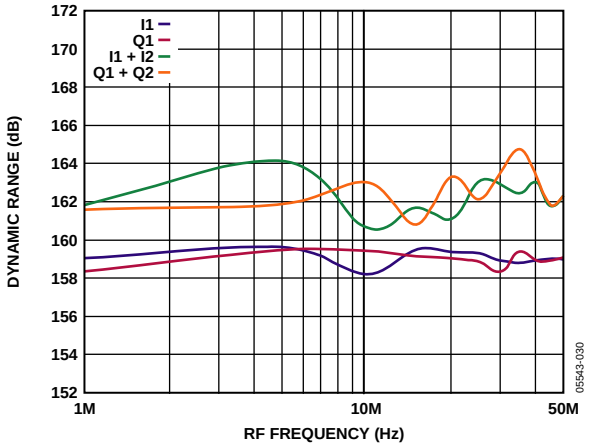


Figure 32. Dynamic Range vs. RF Frequency, IP1dB Minus Noise Level, Single Channel and Two Channels Summed

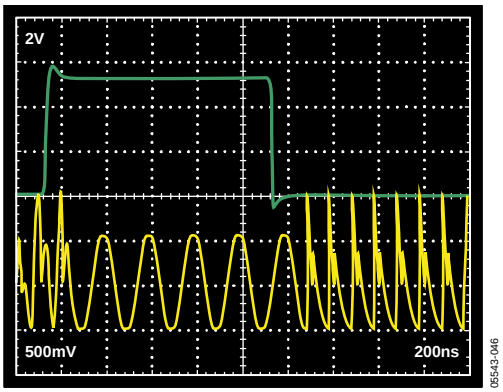


Figure 35. Reset Response—Top: Signal at RSET Pin, Bottom: Output Signal (see Figure 45)

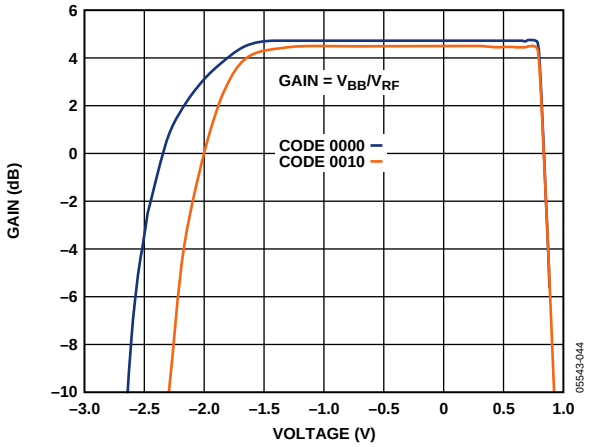


Figure 33. Output Compliance Range (IxPO, QxPO) (see Figure 50)

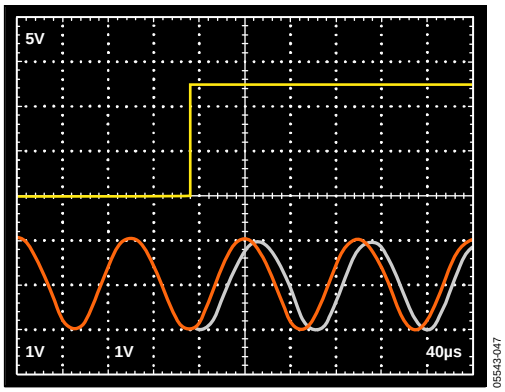


Figure 36. Phase Switching Response—Channel 2 Leads Channel 1 by 45°, Top: Input to PH21, Select Code = 0010; Bottom (Red): Reference Channel 1 I_{OUT}; Bottom (Gray): Channel 2 I_{OUT} Phase Shifted 45°, Channel 1 Reference Phase Select Code = 0000

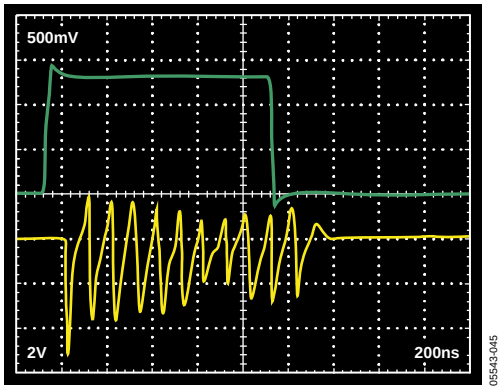


Figure 34. Enable Response—Top: Enable Signal, Bottom: Output Signal (see Figure 44)

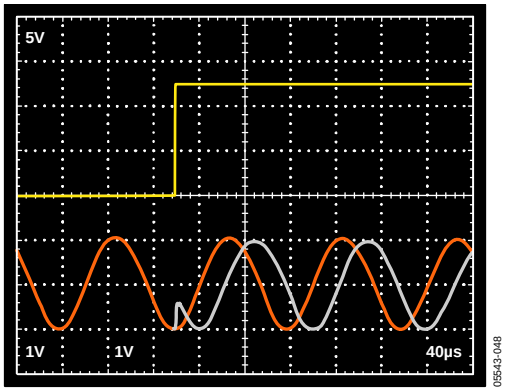


Figure 37. Phase Shifting Response—Channel 2 Leads Channel 1 by 90°, Top: Input to PH21, Select Code = 0100; Bottom (Red): Reference Channel 1 I_{OUT}; Bottom (Gray): Channel 2 I_{OUT} Phase Shifted 90°, Channel 1 Reference Phase Code = 0000

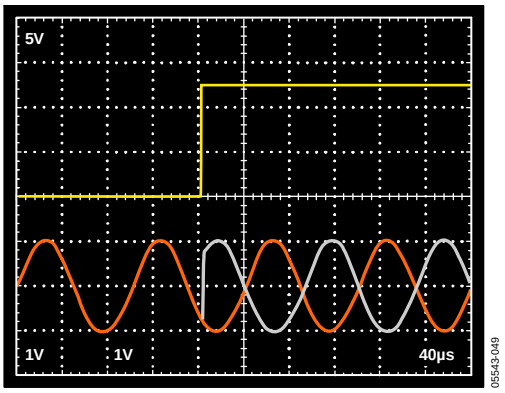


Figure 38. Phase Shifting Response—Channel 2 Leads Channel 1 by 180°, Top: Input to PH23 Select Code = 1000; Bottom (Red): Reference Channel 1 I_{OUT}; Bottom (Gray): Channel 2 I_{OUT} Phase Shifted 180°, Channel 1 Reference Phase Code = 0000

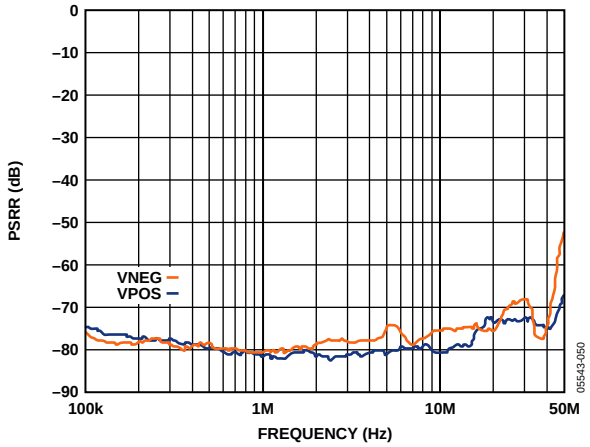


Figure 39. PSRR vs. Frequency (see Figure 51)

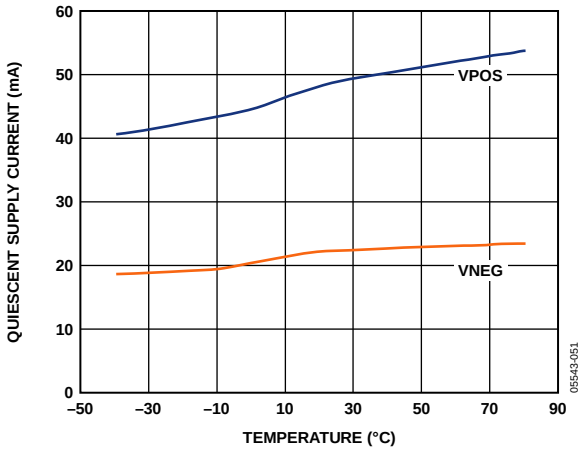


Figure 40. Quiescent Supply Current vs. Temperature

TEST CIRCUITS

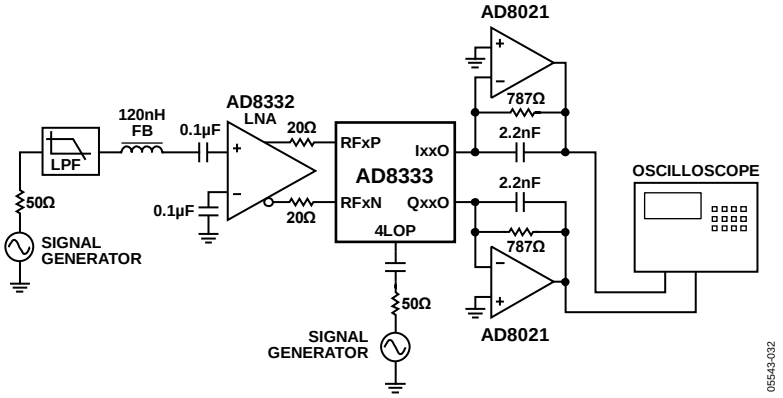


Figure 41. Default Test Circuit

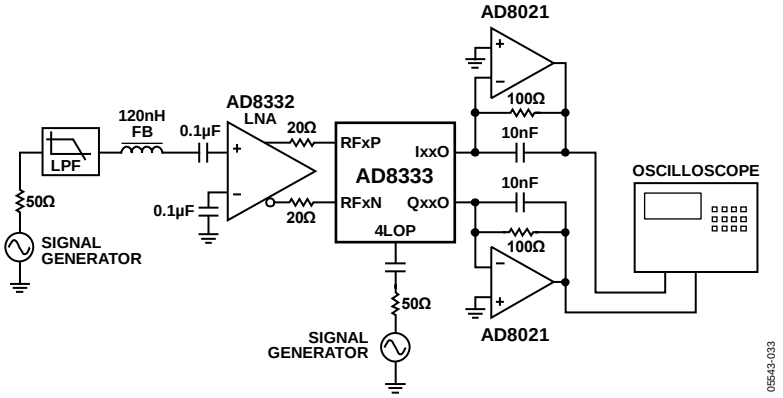


Figure 42. P1dB Test Circuit

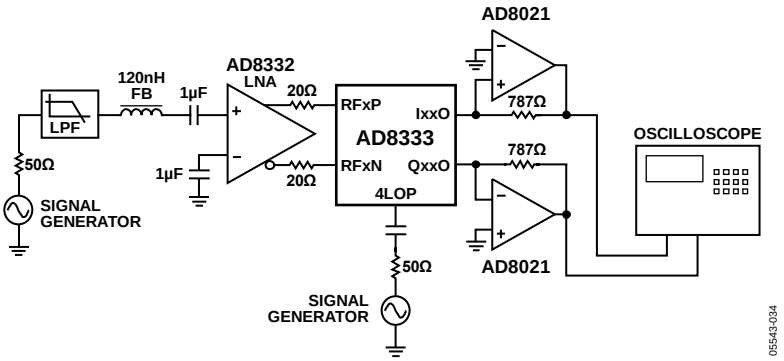


Figure 43. Phase and Amplitude vs. Baseband Frequency

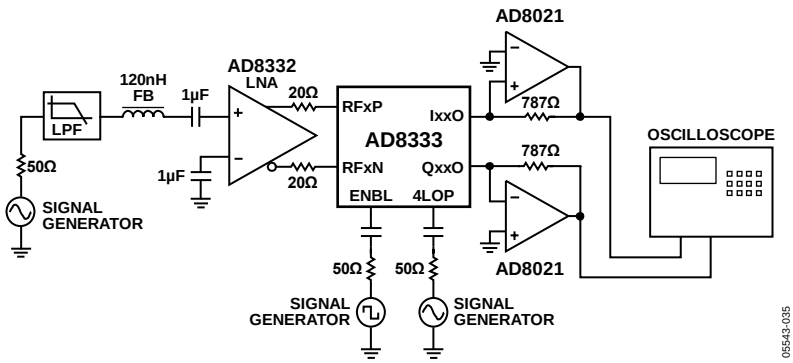


Figure 44. Enable Response

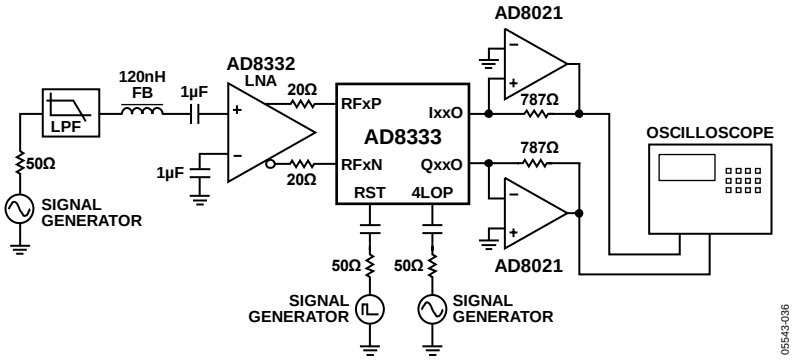


Figure 45. Reset Response

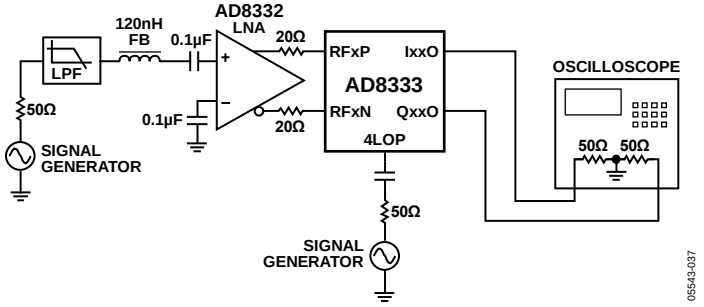


Figure 46. RF Input Range

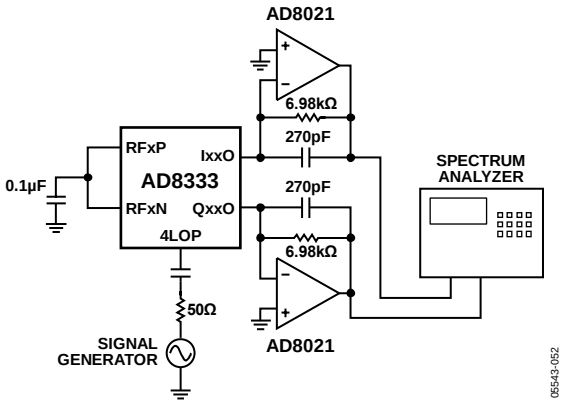


Figure 47. Noise Test Circuit

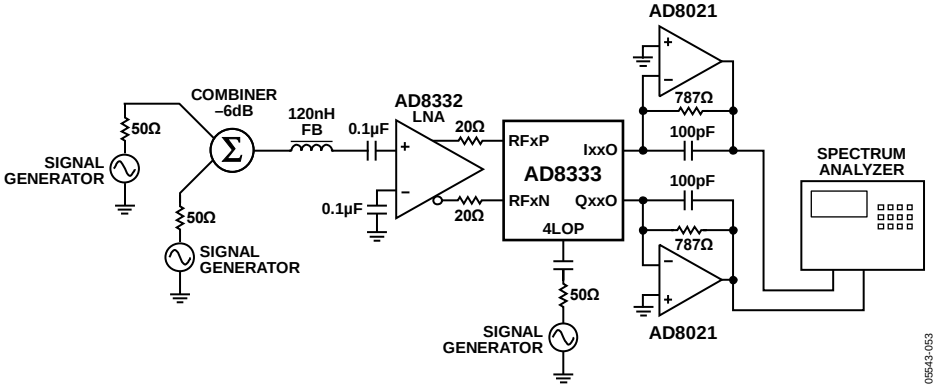


Figure 48. OIP3 vs. Baseband Frequency

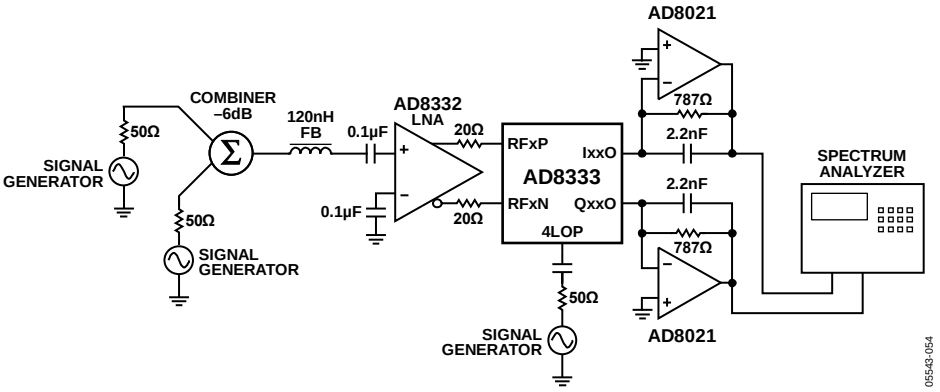


Figure 49. OIP3 and IM3 vs. RF Frequency

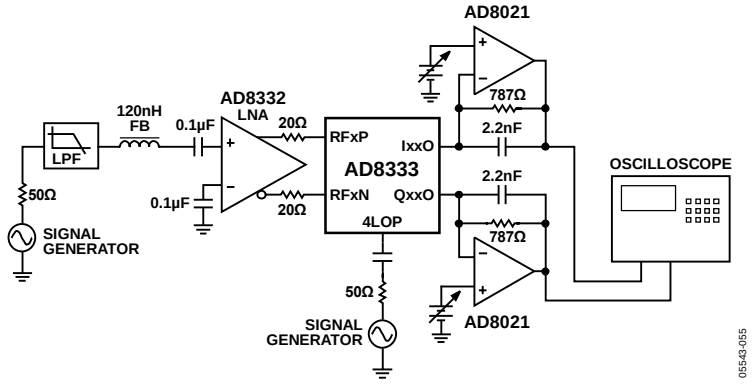


Figure 50. Output Compliance Range

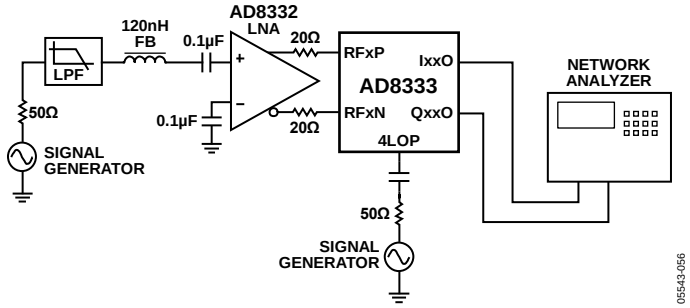


Figure 51. PSRR Test Circuit

THEORY OF OPERATION

The AD8333 is a dual I/Q demodulator with a programmable phase shifter for each channel. The primary applications are phased array beamforming in medical ultrasound, phased array radar, and smart antennae for mobile communications. The AD8333 can also be used in applications that require two well-matched I/Q demodulators.

Figure 52 shows the block diagram and pinout of the AD8333. Three analog and nine quasilogic level inputs are required. Two RF inputs accept signals from the RF sources and a local oscillator (applied to the differential input pins marked 4LOx) common to both channels constitute the analog inputs. Four logic inputs per channel define one of 16 delay states/360° (or 22.5°/step), selectable with PHx0 to PHx3. The reset input is used to synchronize AD8333 devices used in arrays.

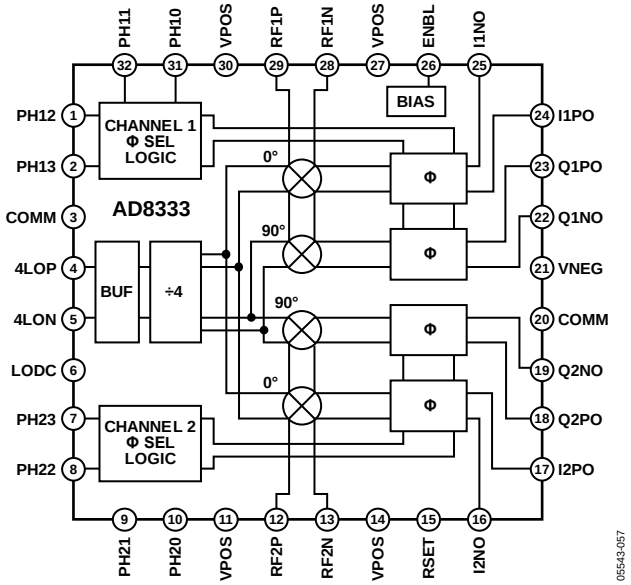


Figure 52. Block Diagram and Pinout

Each of the current formatted I and Q outputs sum together for beamforming applications. Multiple channels are summed and converted to a voltage using a transimpedance amplifier. If desired, channels can also be used individually.

QUADRATURE GENERATION

The internal 0° and 90° LO phases are digitally generated by a divide-by-4 logic circuit. The divider is dc-coupled and inherently broadband; the maximum LO frequency is limited only by its switching speed. The duty cycle of the quadrature LO signals is intrinsically 50% and is unaffected by the asymmetry of the externally connected 4LOx inputs. Furthermore, the divider is implemented such that the 4LOx signals reclock the final flip-flops that generate the internal LO signals and thereby minimizes noise introduced by the divide circuitry.

For optimum performance, the 4LOx inputs are driven differentially but can also be driven in a single-ended fashion. A good choice for a drive is an LVDS device. The common-mode range on each pin is approximately 0.2 V to 3.8 V with nominal ±5 V supplies.

The minimum LO level is frequency dependent (see Figure 22). For optimum noise performance, it is important to ensure that the LO source has very low phase noise (jitter) and adequate input level to ensure stable mixer-core switching. The gain through the divider determines the LO signal level vs. RF frequency. The AD8333 can be operated to very low frequencies at the LO inputs if a square wave is used to drive the LO.

Beamforming applications require a precise channel-to-channel phase relationship for coherence among multiple channels. A reset pin (RSET) is provided to synchronize the 4LOx divider circuits when AD8333 devices are used in arrays. The RSET pin resets the counters to a known state after power is applied to multiple AD8333 devices. A logic input must be provided to the RSET pin when using more than one AD8333. See the Reset Input section for more details.

I/Q DEMODULATOR AND PHASE SHIFTER

The I/Q demodulators consist of double-balanced Gilbert cell mixers. The RF input signals are converted into currents by transconductance stages that have a maximum differential input signal capability of 2.8 V p-p. These currents are then presented to the mixers, which convert them to baseband: RF − LO and RF + LO. The signals are phase shifted according to the code applied to Pin PHx0 to Pin PHx3 (see Table 4). The phase shift function is an integral part of the overall circuit (patent pending). The phase shift listed in Column 1 of Table 4 is defined as being between the baseband I or Q channel outputs. As an example, for a common signal applied to the RF inputs of an AD8333, the baseband outputs are in phase for matching phase codes. However, if the phase code for Channel 1 is 0000 and that of Channel 2 is 0001, Channel 2 leads Channel 1 by 22.5°.

Following the phase shift circuitry, the differential current signal is converted from differential to single ended via a current mirror. An external transimpedance amplifier is needed to convert the I and Q outputs to voltages.

Table 4. Phase Nibble Select Codes

ϕ Shift	PHx3	PHx2	PHx1	PHx0
0°	0	0	0	0
22.5°	0	0	0	1
45°	0	0	1	0
67.5°	0	0	1	1
90°	0	1	0	0
112.5°	0	1	0	1
135°	0	1	1	0
157.5°	0	1	1	1
180°	1	0	0	0
202.5°	1	0	0	1
225°	1	0	1	0
247.5°	1	0	1	1
270°	1	1	0	0
292.5°	1	1	0	1
315°	1	1	1	0
337.5°	1	1	1	1

DYNAMIC RANGE AND NOISE

Figure 53 is an interconnection block diagram of the AD8333. For optimum system noise performance, the RF input signal is provided by a very low noise amplifier, such as the LNA of an AD8332 or the preamplifier of an AD8335. In beamformer applications, the I and Q outputs of a number of receiver channels are summed (for example, the two channels illustrated in Figure 53). The dynamic range of the system increases by the factor 10 $\log_{10}(N)$, where N is the number of channels (assuming random uncorrelated noise). The noise in the two-channel example of Figure 53 is increased by 3 dB while the signal doubles (6 dB), yielding an aggregate SNR improvement of (6 dB − 3 dB) = 3 dB.

Judicious selection of the RF amplifier ensures the least degradation in dynamic range. The input-referred spectral voltage noise density (e_n) of the AD8333 is nominally 9 nV/√Hz to 10 nV/√Hz. For the noise of the AD8333 to degrade the system noise figure (NF) by 1 dB, the combined noise of the source and the LNA must be about twice that of the AD8333, or 18 nV/√Hz. If the noise of the circuitry before the AD8333 is <18 nV/√Hz, the system NF degrades more than 1 dB. For example, if the noise contribution of the LNA and source is equal to the AD8333, or 9 nV/√Hz, the degradation is 3 dB. If the circuit noise preceding the AD8333 is 1.3× as large as that of the AD8333 (or about 11.7 nV/√Hz), the degradation is 2 dB. For a circuit noise of 1.45× that of the AD8333 (13.1 nV/√Hz), the degradation is 1.5 dB.

To determine the input-referred noise, it is important to know the active low-pass filter (LPF) values R_{FILT} and C_{FILT}, shown in Figure 53. Typical filter values (for example, those used on the evaluation board) are 787 Ω and 2.2 nF and implement a 90 kHz single-pole LPF. If the RF and LO are offset by 10 kHz, the demodulated signal is 10 kHz and is passed by the LPF. The single-channel mixing gain from the RF input to the AD8021 output (for example, ΣI, ΣQ) is approximately 1.7 × 4.7 dB. This together with the 9 nV/√Hz AD8333 noise results in about 15.3 nV/√Hz at the AD8021 output. Because the AD8021, including the 787 Ω feedback resistor, contributes another 4.4 nV/√Hz, the total output-referred noise is about 16 nV/√Hz. This value can be adjusted by increasing the filter resistor while maintaining the corner frequency, thereby increasing the gain. The factor limiting the magnitude of the gain is the output swing and drive capability of the operational amplifier selected for the I-to-V converter, in this instance the AD8021.

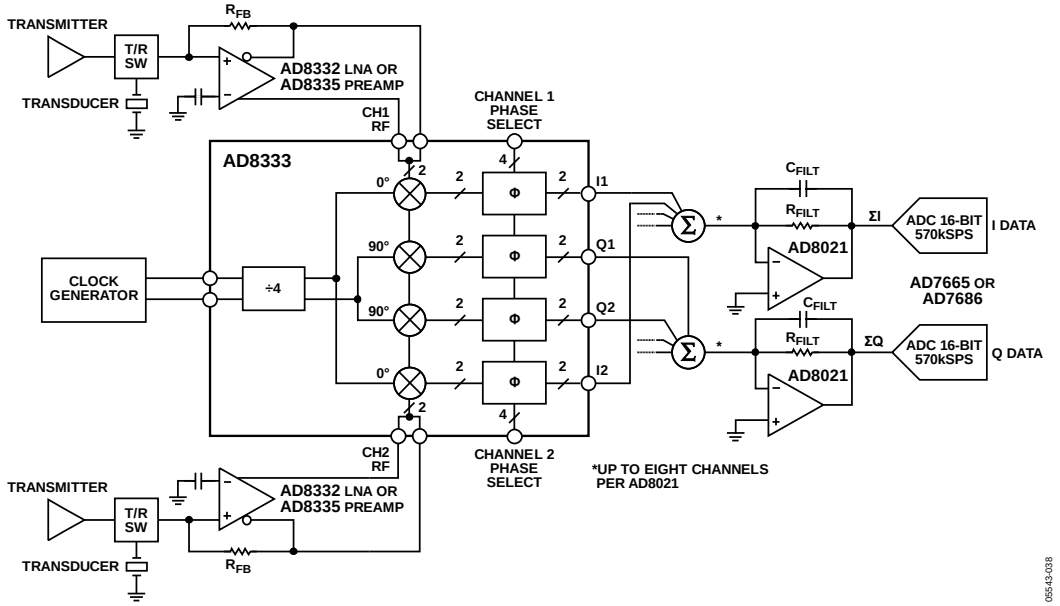


Figure 53. Interconnection Block Diagram

SUMMATION OF MULTIPLE CHANNELS (ANALOG BEAMFORMING)

Beamforming, as applied to medical ultrasound, is defined as the phase alignment and summation of signals generated from a common source but received at different times by a multielement ultrasound transducer. Beamforming has two functions: it imparts directivity to the transducer, enhancing its gain, and it defines a focal point within the body from which the location of the returning echo is derived. The primary application for the AD8333 is in analog beamforming circuits for ultrasound.

PHASE COMPENSATION AND ANALOG BEAMFORMING

Modern ultrasound machines used for medical applications employ a 2^n binary array of receivers for beamforming, with typical array sizes of 16 or 32 receiver channels phase-shifted and summed together to extract coherent information. When used in multiples, the desired signals from each of the channels can be summed to yield a larger signal (increased by a factor N, where N is the number of channels), while the noise is increased by the square root of the number of channels. This technique enhances the signal-to-noise performance of the machine. The critical elements in a beamformer design are the means to align the incoming signals in the time domain and the means to sum the individual signals into a composite whole.

In traditional analog beamformers incorporating Doppler, a V-to-I converter per channel and a crosspoint switch precede passive delay lines used as a combined phase shifter and summing circuit. The system operates at the receive frequency (RF) through the delay line, and then the signal is down-converted by a very large dynamic range I/Q demodulator.

The resultant I and Q signals are filtered and sampled by two high resolution ADCs. The sampled signals are processed to extract the relevant Doppler information.

Alternatively, the RF signal can be processed by downconversion on each channel individually, phase shifting the downconverted signal and then combining all channels. The AD8333 provides the means to implement this architecture. The downconversion is done by an I/Q demodulator on each channel, and the summed current output is the same as in the delay line approach. The subsequent filters after the I-to-V conversion and the ADCs are similar.

The AD8333 integrates the phase shifter, frequency conversion, and I/Q demodulation into a single package and directly yields the baseband signal. To illustrate this, Figure 54 is a simplified diagram showing two channels. The ultrasound wave (USW) is received by two transducer elements, TE1 and TE2, in an ultrasound probe and generates the E1 and E2 signals. In this example, the phase at TE1 leads the phase at TE2 by 45°.

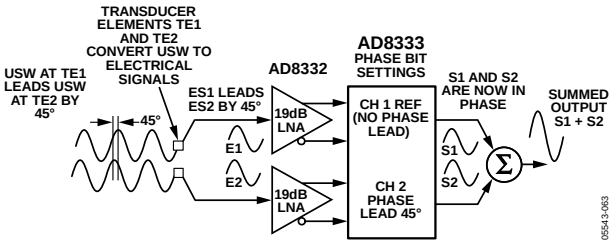


Figure 54. Simplified Example of the AD8333 Phase Shifter

In a real application, the phase difference depends on the element spacing, λ (wavelength), speed of sound, angle of incidence, and other factors. The ES1 and ES2 signals are amplified 19 dB by the low noise amplifiers in the AD8332. For optimum signal-to-noise performance, the output of the LNA is applied directly to the input of the AD8333. To sum the ES1 and ES2 signals, ES2 is shifted 45° relative to ES1 by setting the phase code in Channel 2 to 0010. The phase-aligned current signals at the output of the AD8333 are summed in an I-to-V converter to provide the combined output signal with a theoretical improvement in dynamic range of 3 dB for the sum of two channels.

CHANNEL SUMMING

In a beamformer using the AD8333, the bipolar currents at the I and Q outputs are summed directly. Figure 55 illustrates 16 summed channels (for clarity, these channels are shown as current sources) as an example of an active current summing circuit using the AD8333. This figure also illustrates the AD8021 as first-order current summing circuits and AD797 devices as low noise second-order summing circuits. Beginning with the operational amplifiers, there are a few important considerations in the circuit shown in Figure 55.

The operational amplifiers selected for the first-order summing amplifiers must have good frequency response over the full operating frequency range of the AD8333 devices and be able to source the current required at the AD8333 I and Q outputs.

The total current of each AD8333 is 6.6 mA for the multiples of the 45° phase settings (Code 0010, Code 0110, Code 1010, and Code 1110) and is divided nearly equally between the baseband frequencies (including a dc component) and the second harmonic of the local oscillator frequency. The desired CW signal tends to be much less (<40 dB) than the unwanted interfering signals.

When determining the large signal requirements of the first-order summing amplifiers and low-pass filters, the very small CW signal can be ignored. The number of channels that can be summed is limited by the output drive current capacity of the operational amplifier selected: 60 mA to 70 mA for a linear output current for ±5 V and ±12 V, respectively, for the AD8021. Because the AD8021 implements an active LPF together with R1x and C1x, it must absorb the worst-case current provided by the AD8333, for example, 6.6 mA. Therefore, the maximum number of channels that the AD8021 can sum is 10 for ±12 V or eight for ±5 V supplies. In practical applications, CW channels are used in powers of two, thus the maximum number per AD8021 is eight.

Another consideration for the operational amplifier selected as an I-to-V converter is the compliance voltage of the AD8333 I and Q outputs. The maximum compliance voltage is 0.5 V, and a dc bias must be provided at these pins. The AD8021 active LPF satisfies these requirements; it keeps the outputs at 0 V via the virtual ground at the operational amplifier inverting input while providing any needed dc bias current.

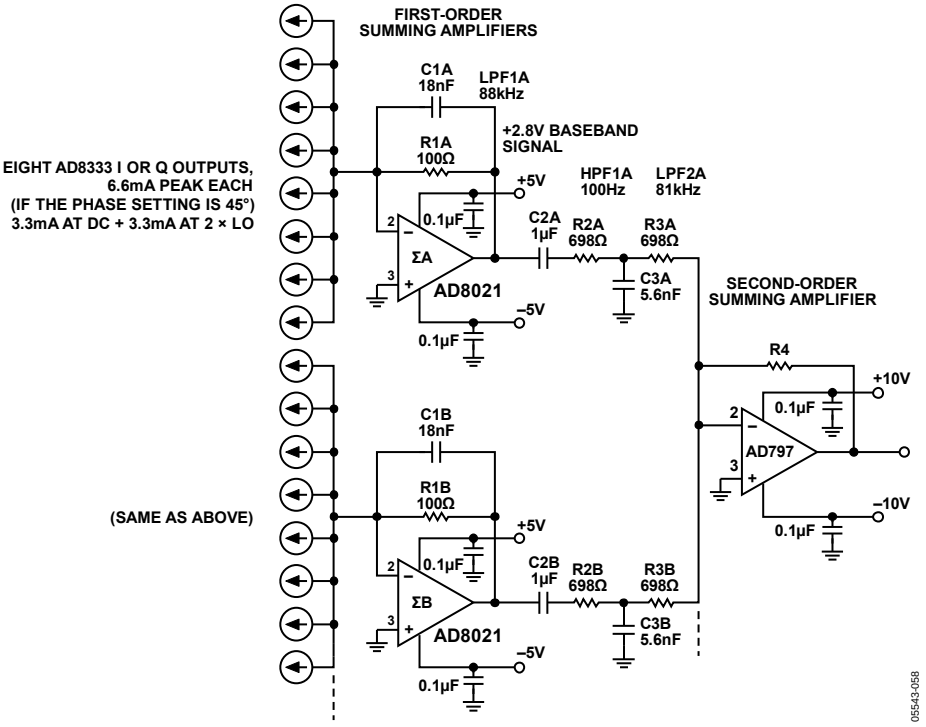


Figure 55. A 16-Channel Beamformer

As previously noted, a typical CW signal has a large dc and very low frequency component compared with its desired low CW Doppler baseband frequency, and another unwanted component at the 2 × LO. The dc component flows through the gain resistors R1x, and the 2 × LO flows through the capacitors C1x. The smaller desired CW Doppler baseband signal is in the frequency range of 1 kHz to 50 kHz.

Because the output current of the AD8333 contains the baseband frequency, a dc component, and the 2 × LO frequency voltages, the desired small amplitude baseband signal must be extracted after a series of filters. These are shown in Figure 55 as LPFnA, HPFnA, and gain stages.

Before establishing the value of C_{LPF1}, the resistor R_{LPF1} is selected based on the peak operating current and the linear range of the operational amplifier. Because the peak current for each AD8333 is 6.6 mA and there are eight channels to be summed, the total peak current required is 52.8 mA. Approximately half of this current is dc, and the other half is at a frequency of 2 × LO. Therefore, about 26.4 mA flows through the resistor, and the remaining 26.4 mA flows through the capacitor. R1 was selected as 100 Ω and, after filtering, generates a peak dc and very low frequency voltage of 2.64 V at the AD8021 output. For power supplies of ±5 V, 100 Ω is a good choice for R1.

However, because the CW signal needs to be amplified as much as possible and the noise degradation of the signal path minimized, the value of R1 must be as large as possible. A larger supply helps in this regard, and the only factor limiting the largest supply voltage is the required power.

For a ±10 V supply on the AD8021, R1 can be increased to 301 Ω to realize the same headroom as with a ±5 V supply. If a higher value of R1 is used, C1 must be adjusted accordingly (in this example, 1/3 the value of the original value) to maintain the desired LPF roll-off. The principal advantage of a higher supply is greater dynamic range, and the trade-off is power consumption. The user must weigh the trade-offs associated with the supply voltage, R1, C1, and the following circuitry. A suggested design sequence is as follows:

Select a low noise, high speed operational amplifier. The spectral density noise (e_n) must be <2 nV/√Hz, and the 3 dB bandwidth must be ≥3× the expected maximum 2 × LO frequency.

Divide the maximum linear output current by 6.6 mA to determine the maximum number of AD8333 channels that can be summed.

Select the largest value of R1 that permits the output voltage swing within the power supply rails.

Calculate the value of C1 to implement the LPF corner that allows the CW Doppler signal to pass with maximum attenuation of the 2 × LO signal.

The filter LPF1A establishes the upper frequency limit of the baseband frequency and is selected well below the 2 × LO frequency, typically 100 kHz or less (for example, 88 kHz in Figure 55).

A useful equation for calculating C1 is

$$C1 = \frac{1}{2\pi R1 f_{LPF1}} \quad (1)$$

As previously mentioned, the AD8333 output current contains a dc current component. This dc component is converted to a large dc voltage by the AD8021 LPF. Capacitor C2 filters this dc component and, with R2 + R3, establishes a high-pass filter with a low frequency cutoff of about 100 Hz. Capacitor C3 is much smaller than C2 and, consequently, can be neglected. C2 can be calculated by

$$C2 = \frac{1}{2\pi (R2 + R3) f_{HPF1}} \quad (2)$$

To achieve maximum attenuation of the 2 × LO frequency, a second low-pass filter, LPF2, is established using the parallel combination of R2 and R3, and C3. Its −3 dB frequency is

$$f_{LPF2} = \frac{1}{2\pi (R2 \,||\, R3) C3} \quad (3)$$

In the example shown in Figure 55, f_{LPF2} = 81 kHz.

Finally, the feedback resistor of the AD797 must be calculated. This is a function of the input current (number of channels) and the supply voltage.

The second-order summing amplifier requires a very low noise operational amplifier, such as the AD797, with 0.9 nV/√Hz, because the amplifier gain is determined by Feedback Resistor R4 divided by the parallel combination of the LPF2A resistors seen looking back toward the AD8021 devices. Referring to Figure 55, the AD797 in-band (100 Hz to 88 kHz) gain is expressed as

$$\frac{R4}{\left[(R2A + R3A) \,||\, (R2B + R2B)\right]} \quad (4)$$

The AD797 noise gain can increase to unacceptable levels because the denominator of the gain equation is the parallel resistance of all the R2 + R3 resistors in the AD8021 outputs. For example, for a 64-channel beamformer, the resistance seen looking back toward the AD8021 devices is about 1.4 kΩ/8 = 175 Ω. For this reason, the value of (R2x + R3x) must be as large as possible to minimize the noise gain of the AD797. (Note that this is the case for the AD8021 stages because they look back into the high impedance current sources of the AD8333 devices.)

Due to these considerations, it is advantageous to increase the gain of the AD8021 devices as much as possible because the value of (R2x + R3x) can be increased proportionally. Resistors (R2x + R3x) convert the CW voltages to currents that are summed at the inverting inputs of the AD797 operational amplifier, and then amplified and converted to voltages by R4.

The value of R4 needs to be chosen iteratively as follows:

1. Determine the number of AD8021 first-order summing amplifiers. In Figure 55, there are two; for a 32-channel beamformer, there must be four, and for a 64-channel beamformer, there must be eight.
2. Determine the output noise from the AD8021 devices. A first-order calculation can be based on a value of AD8333 output current noise of about 20 pA/√Hz. For the values in Figure 55, this results in about 6 nV/√Hz for eight channels after the AD8021 devices. Adding the noise of the AD8021 and the 100 Ω feedback resistor results in about 6.5 nV/√Hz total noise after the AD8021 LPF in the CW Doppler band.
3. Determine the noise of the circuitry after the AD797 and determine the desired signal level.
4. Determine the voltage and current noise of the second-order summing amplifiers.
5. Choose a value for (R2x + R3x) and for R4. Determine the resulting output noise after the AD797 for one channel, and then multiply this value by the square root of the number of summed AD8021 devices. Next, check AD797 output noise (both current and voltage noise). Ideally, the sum of the noise of the resistors and the AD797 must be less than a factor of 3 than the noise due to the AD8021 outputs.
6. Check the following stages output noise against the calculated noise from the combiner circuit and AD8333 devices. Ideally, the noise from the following stage must be less than 1/3 of the calculated noise.
7. If the combined noise is too large, experiment with increasing/decreasing values for (R2x + R3x) and R4.

To simplify, the user can also simulate or build a combiner circuit for optimum performance. It must be noted that the ~20 pA/√Hz output from the AD8333 is for the AD8333 with shorted RF inputs. In an actual system, the current noise output from the AD8333 is most likely dominated by the noise from the AD8332 LNA and the noise from the source and other circuitry before the LNA. This helps ease the design of the combiner. The preceding procedures for determining the optimum values for the combiner are based on the noise floor of the AD8333 only.

As an example, for a 32-channel beamformer using four low-pass filters, as shown in Figure 55, (R2x + R3x) = 1.4 kΩ and R4 = 6.19 kΩ. The theoretical noise increase of √N is degraded by only about 1 dB.

DYNAMIC RANGE INFLATION

Although all 64 channels can theoretically be summed together at a single amplifier, it is important to realize that the dynamic range of the summed output increases by 10 $\log_{10}$(N) if all channels have uncorrelated noise, where N is the number of channels to be summed.

The summed signal level increases by a factor of N, whereas the noise increases only as √N. In the case of 64 channels, this is an increase in dynamic range of 18 dB. Note that the AD8333 dynamic range is already about 160 dB/Hz; the summed dynamic range is 178 dB/Hz (equivalent to about 29.5 bits/Hz). In a 50 kHz noise bandwidth, this is 131 dB (21.7 bits).

DISABLING THE CURRENT MIRROR AND DECREASING NOISE

The noise contribution of the AD8333 can potentially be reduced if the current mirrors that convert the internal differential signals to single-ended signals are bypassed (see Figure 56). Current mirrors interface to the AD8021 I-V converters shown in Figure 53, and output capacitors across the positive and negative outputs provide low-pass filtering. The AD8021 devices force the AD8333 output voltage to 0 V and then process the bipolar output current; however, the internal current mirrors introduce a significant amount of noise. This noise can be reduced if the mirrors are disabled and the outputs are externally biased.

The mirrors are disabled by connecting VNEG to ground and providing external bias networks, as shown in Figure 56. The larger the drop across the resistors, the less noise they contribute to the output; however, the voltage on the I and Q output nodes cannot exceed 0.5 V. Voltages exceeding approximately 0.7 V turn on the PNP devices and forward bias the ESD protection diodes. Inductors provide an alternative to resistors, enabling reduced static power by eliminating the power dissipation in the bias resistors.

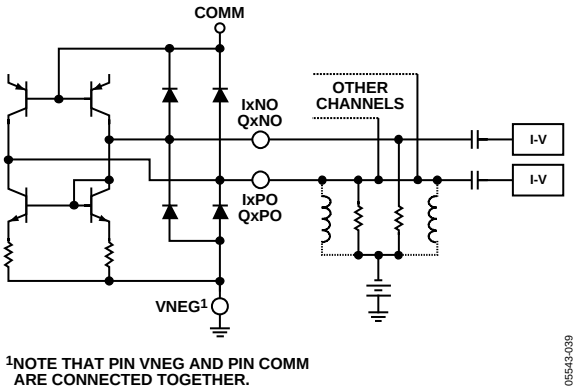


Figure 56. Bypassing the Internal Current Mirrors

With inductors, the main limitation might be low frequency operation, as is the case in CW Doppler in ultrasound where the frequency range of interest goes from a few hundred hertz to about 30 kHz. In addition, it is still important to provide enough gain through the I-to-V circuitry to ensure that the bias resistor and I-to-V converter noise do not contribute significantly to the noise from the AD8333 outputs. Another approach is to provide a single external current mirror that combines all channels; it is also possible to implement a high-pass filter with this circuit to help with offset and low frequency reduction.

The main disadvantage of the external bias approach is that two I-V amplifiers are needed because of the differential output (see Figure 56). For beamforming applications, the outputs are still summed, but there is twice the number of lines. Only two bias resistors are needed for all outputs that are connected together. The resistors are scaled by dividing the value of a single output bias resistor through N, the number of channels connected in parallel. The bias current depends on the phase selected: for phase 0°, it is about 2.5 mA per side, whereas in the case of 45°, it is about 3.5 mA per side. The bias resistors must be chosen based on the larger bias current value of 3.5 mA and the chosen VNEG. VNEG must be at least −5 V and can be larger for additional noise reduction.

Excessive noise or distortion at high signal levels degrades the dynamic range of the signal. Transmitter leakage and echoes from slow moving tissue generate the largest signal amplitudes in ultrasound CW Doppler mode and are largest near dc and at low frequencies. A high-pass filter introduced immediately following the AD8333 reduces the dynamic range. This is shown by the two coupling capacitors after the external bias resistors in Figure 56. Users have to determine what is acceptable for a particular application. Care must be taken in designing the external circuitry to avoid introducing noise via the external bias and low frequency reduction circuitry.

APPLICATIONS INFORMATION

The AD8333 is the key component of a phase-shifter system that aligns time-skewed information contained in RF signals. Combined with a variable gain amplifier (VGA) and low noise amplifier (LNA), the AD8333 forms a complete analog receiver for a high performance ultrasound system. Figure 57 is a block diagram of a complete receiver using the AD8333, AD8331, AD8332, and AD8334.

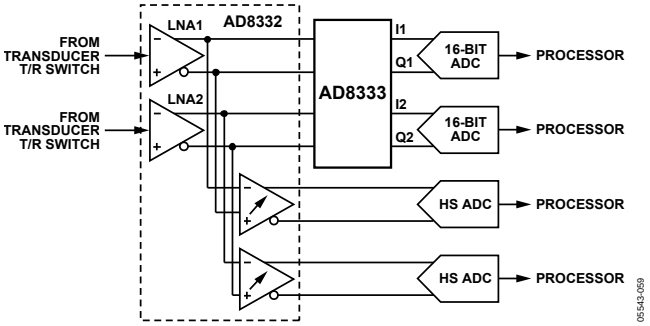


Figure 57. Block Diagram—Ultrasound Receiver Using the AD8333 and AD8332 LNA

As a major element of an ultrasound system, it is important to consider the many input/output options of the AD8333 that are necessary to perform its intended function. Figure 61 shows the basic connections.

LOGIC INPUTS AND INTERFACES

The logic inputs of the AD8333 are all bipolar-level sensitive inputs. They are not edge triggered, nor are they to be confused with classic TTL or other logic family input topologies. The voltage threshold for these inputs is VPOS × 0.3, so for a 5 V supply the threshold is 1.5 V, with a hysteresis of ±0.2 V. Although the inputs are not of themselves logic inputs, any 5 V logic family can drive them.

RESET INPUT

The RSET pin is used to synchronize the LO dividers in AD8333 arrays. Because they are driven by the same internal LO, the two channels in any AD8333 are inherently synchronous. However, when multiple AD8333 devices are used, it is possible that their dividers wake up in different phase states. The function of the RSET pin is to phase align all the LO signals in multiple AD8333 devices.

The 4 × LO divider of each AD8333 can initiate in one of four possible states: 0°, 90°, 180°, or 270°. The internally generated I/Q signals of each AD8333 LO are always at a 90° angle relative to each other, but a phase shift can occur during power-up between the internal LOs of the different AD8333 devices.

The RSET pin provides an asynchronous reset of the LO dividers by forcing the internal LO to hang. This mechanism also allows the measurement of nonmixing gain from the RF input to the output.

The rising edge of the active high RSET pulse can occur at any time, but the duration must be ≥300 ns minimum (t_{PW-MIN}). When the RSET pulse transitions from high to low, the LO dividers are reactivated; however, there is a short delay until the divider recovers to a valid state. To guarantee synchronous operation of an array of AD8333 devices, the 4 × LO clock must be disabled when the RSET transitions high, and then remain disabled for at least 300 ns after RSET transitions low.

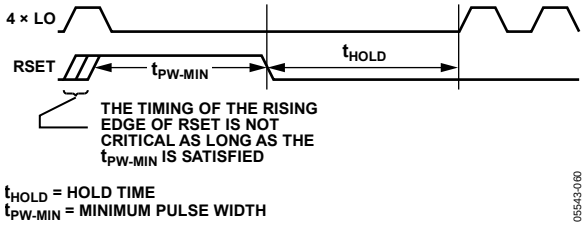


Figure 58. Timing of the RSET Signal to 4 × LO

Synchronization of multiple AD8333 devices can be checked as follows:

1. Set the phase code of all AD8333 channels to the same setting, for example, 0000.
2. Apply a test signal to a single channel that generates a sine wave in the baseband output, and then measure the output.
3. Apply the same test signal to all channels simultaneously, and then measure the output.

Because all the phase codes of the AD8333 devices are the same, the combined signal must be N times bigger than the single channel. The combined signal is less than N times one channel if any of the LO phases of individual AD8333 devices are in error.

CONNECTING TO THE LNA OF THE AD8331/AD8332/AD8334/AD8335 VGAs

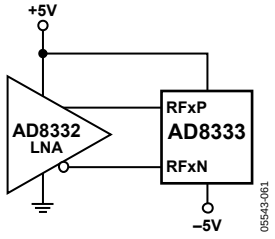


Figure 59. Connecting the AD8333 to the LNA of an AD8332

The RFxx inputs (Pin 12, Pin 13, Pin 28, and Pin 29) are optimized for maximum dynamic range when dc-coupled to the differential output pins of the LNA of the AD8331/AD8332/AD8334 or the AD8335 series of VGAs and can be connected directly, as shown in Figure 59.

INTERFACING TO OTHER AMPLIFIERS

If amplifiers other than the AD8332 LNA are connected to the input, attention must be paid to their bias and drive levels. For maximum input signal swing, the optimum bias level is 2.5 V, and the RF input must not exceed 5 V to avoid turning on the ESD protection circuitry. If ac coupling is used, a bias circuit, such as that illustrated in Figure 60, is recommended. An internal bias network is provided; however, additional external biasing can center the RF input at 2.5 V.

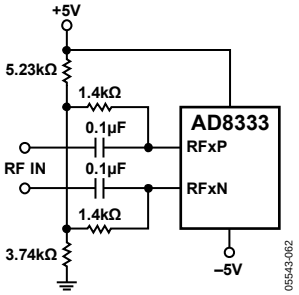


Figure 60. AC Coupling the AD8333 RF Input

To realize the full range of performance, the AD8333 must be driven from a differential source. Using a single-ended source is strongly discouraged because of internal supply headroom constraints.

LO INPUT

The LO input is a high speed, fully differential analog input that responds to differences in the input levels, not in the logic levels. The LO inputs can be driven with a low common-mode voltage amplifier, such as the National Semiconductor DS90C401 LVDS driver.

Figure 22 and Figure 23 show the range of common-mode voltages and useable LO levels when the LO input is driven with a single-ended sine wave. Logic families, such as TTL or CMOS, are unsuitable for direct coupling to the LO input.

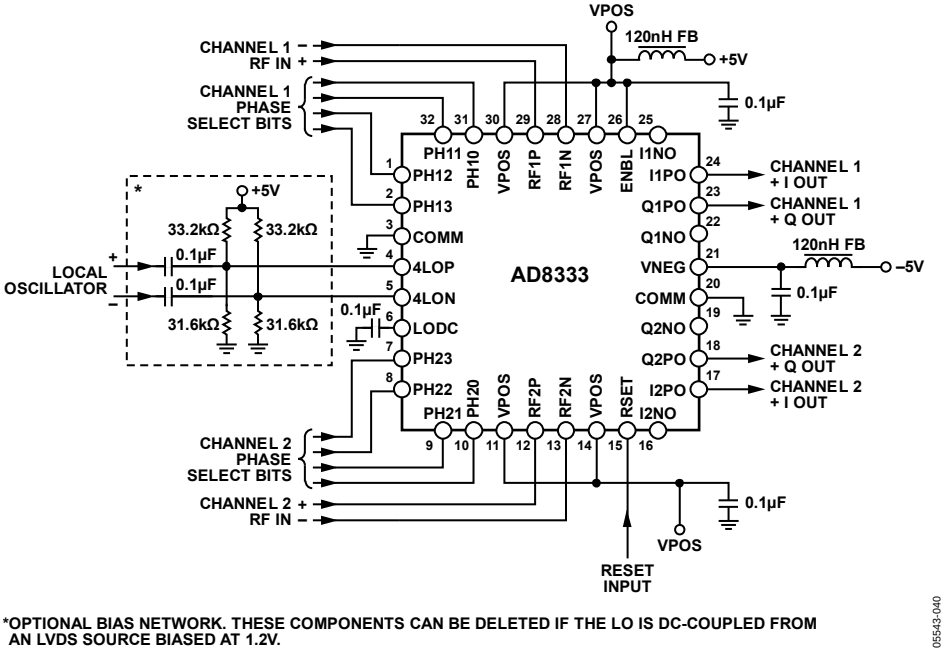


Figure 61. AD8333 Basic Connections

EVALUATION BOARD

The AD8333-EVALZ evaluation board provides a platform for test and evaluation of the AD8333 I/Q demodulator and phase shifter. The board is shipped fully assembled and tested and is signal ready. A pair of AD8332 low-noise amplifiers (LNA) provide input matching and amplification for the differential input of the AD8333. A photograph of the board is shown in Figure 62 and a schematic diagram is shown in Figure 64. The board requires dual 5 V supplies capable of supplying 300 mA or greater. Except for the optional components shown in grayscale, the board is completely built and tested.

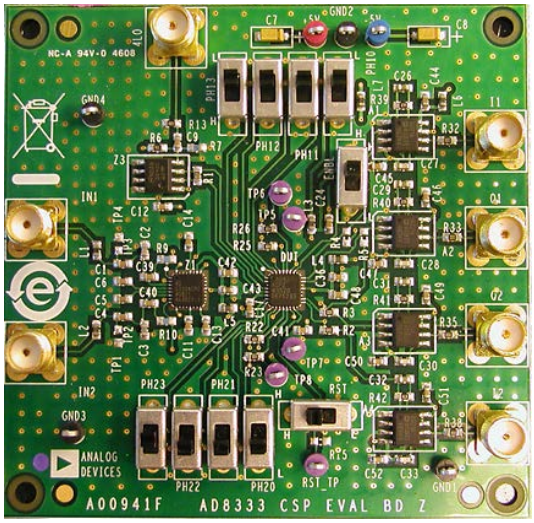


Figure 62. Evaluation Board (Actual Size)

FEATURES AND OPTIONS

The evaluation board has several user-configurable features and options. Table 5 lists the configuration switches and their functions.

Table 5. Switch Functions

Switch	Function	Configuration
ENBL	Enable or disable the AD8333	Bottom = disable; top = enable
PH10	Channel 1 Phase Bit 0 (LSB)	Top = 0; bottom = 1
PH11	Channel 1 Phase Bit 1	Top = 0; bottom = 1
PH12	Channel 1 Phase Bit 2	Top = 0; bottom = 1
PH13	Channel 1 Phase Bit 3 (MSB)	Top = 0; bottom = 1
PH20	Channel 2 Phase Bit 0 (LSB)	Top = 1; bottom = 0
PH21	Channel 2 Phase Bit 1	Top = 1; bottom = 0
PH22	Channel 2 Phase Bit 2	Top = 1; bottom = 0
PH23	Channel 2 Phase Bit 3 (MSB)	Top = 1; bottom = 0
RST	Reset	Left = run; right = reset

Phase Nibble

The phase nibble configures the phase delay for each channel in sixteen 22.5° increments from 0° to 337.5°. The increments increase proportionally in a simple binary format from 0H (hexadecimal) to FH. Table 4 lists the phase shift and corresponding code for each bit. The bits are labeled 0 and 1, corresponding to low and high, respectively, on the silkscreen. The switches select the desired state.

Enable and Reset Switches

For normal operation, place a switch in the upper position of ENBL. To disable the AD8333, move the switch to the lower position. For normal operation, the switch for RST is in its right position. When the switch is in the left position, the device counter is held in reset and no mixing occurs.

Fixed Options

Several options can be realized by adding or changing resistors.

LNA Input Impedance

The shipping configuration of the input impedance of the LNA is 50 Ω to match the output impedance of most signal generators. Input impedances up to 6 kΩ are obtained by selecting the R9 and R10 values. Details concerning this circuit feature are found in the AD8332 data sheet. For reference, Table 6 lists common values of input impedance and corresponding feedback resistor values.

Table 6. LNA External Component Values for Typical Values of Source Impedance

R_{IN} (Ω)	R_{FB}, Nearest STD 1% Value (Ω)	C_{SH} (pF)
50	280	22
75	412	12
100	562	8
200	1.13 k	1.2
500	3.01 k	None
6 k	∞	None

Current Summing

The output transimpedance amplifiers, A1 through A4, are configured as I-to-V converters to convert the output current of the AD8333 to a voltage. The low-pass filters formed by the feedback components are designed for single-channel operation with ±5 V supplies.

Optional Resistors R4 and R5 sum the two channels. With R4 and R5 installed, R2 and R3 are removed, and then the sum of the outputs is seen at the I1xO and Q1xO output SMA connectors.

The user has the option to adjust the values of R39, R40, R41, or R42 according to the power supply voltages and expected input current levels. For the same supply voltages, if two channels are summed together, the feedback resistors are halved and the filter capacitor values doubled to optimize the output swing.

Filter Capacitors C26, C29, C31, and C 32 establish the roll-off characteristic according to the following well-known equation:

$$f = \frac{1}{\omega RC}$$

where *R* is the value of R39, R40, R41, or R42, and *C* is the value of C26, C29, C31, or C32.

Reset Input

For normal operation, the reset input is high (no reset). To drive the reset with a dynamic signal, a provision is made to connect a signal generator at the RST input. A 49.9 Ω, 0603 surface-mount resistor can be installed at R15 to terminate the reset input for pulsed experiments. In this configuration, the switch at RST is not used and must be removed to avoid loading the power supply.

MEASUREMENT SETUP

Figure 63 is a layout of the AD8333-EVALZ showing the connectors and switches. Figure 65 shows a typical board and test equipment setup with two signal generators, a power splitter, and a ±5 V, 300 mA (minimum) power supply.

For ease in observing waveforms, the signal generators can be synchronized. Remember that the f_{4LO} signal generator frequency is four times that of the nominal frequency of the RF source. For example, to detect signals with a nominal center frequency of 5 MHz, an f_{4LO} frequency of 20 MHz is applied to the oscillator input. For an applied RF signal of 5.01 MHz, the mix frequencies are 10 kHz and 10.01 MHz. Because of the low-pass active filter of the transconductance amplifiers (A1 through A4), the 10.01 MHz component is suppressed, and only the 10 kHz is observed at the output.

Take care to avoid overdriving the LNA input of the AD8332. The LNA gain is 19 dB (9.5×) and the maximum output swing must not be exceeded; −10 dBm suffices for many experiments. The f_{4LO} input is ac-coupled to a 5 V LVDS buffer to provide an ideal interface to the AD8333.

The f_{4LO} level is frequency dependent; refer to Figure 22 for minimum signal levels, and then adjust the generator output level accordingly.

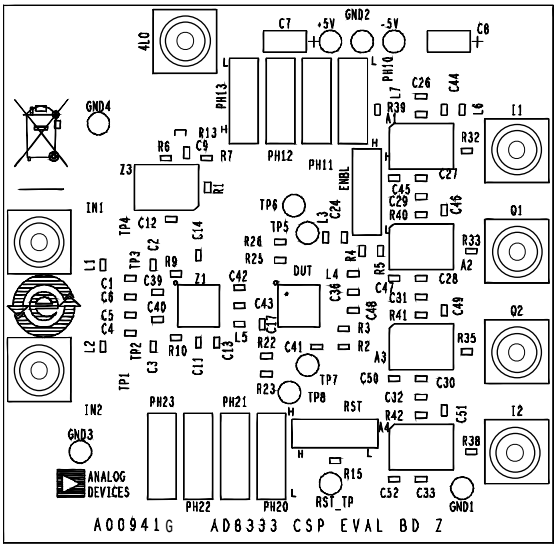


Figure 63. Evaluation Board Assembly

EVALUATION BOARD SCHEMATIC AND ARTWORK

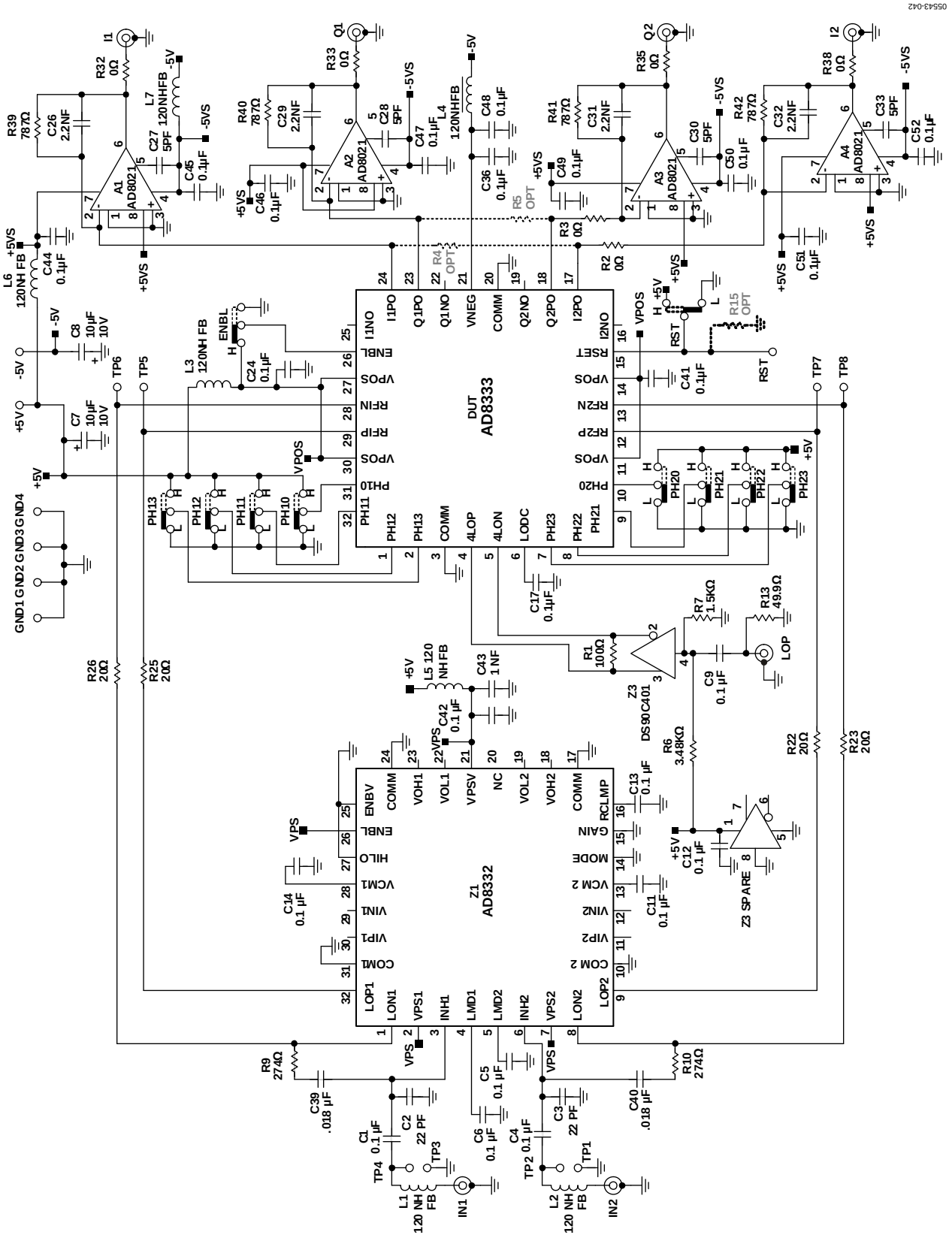


Figure 64. Evaluation Board Schematic

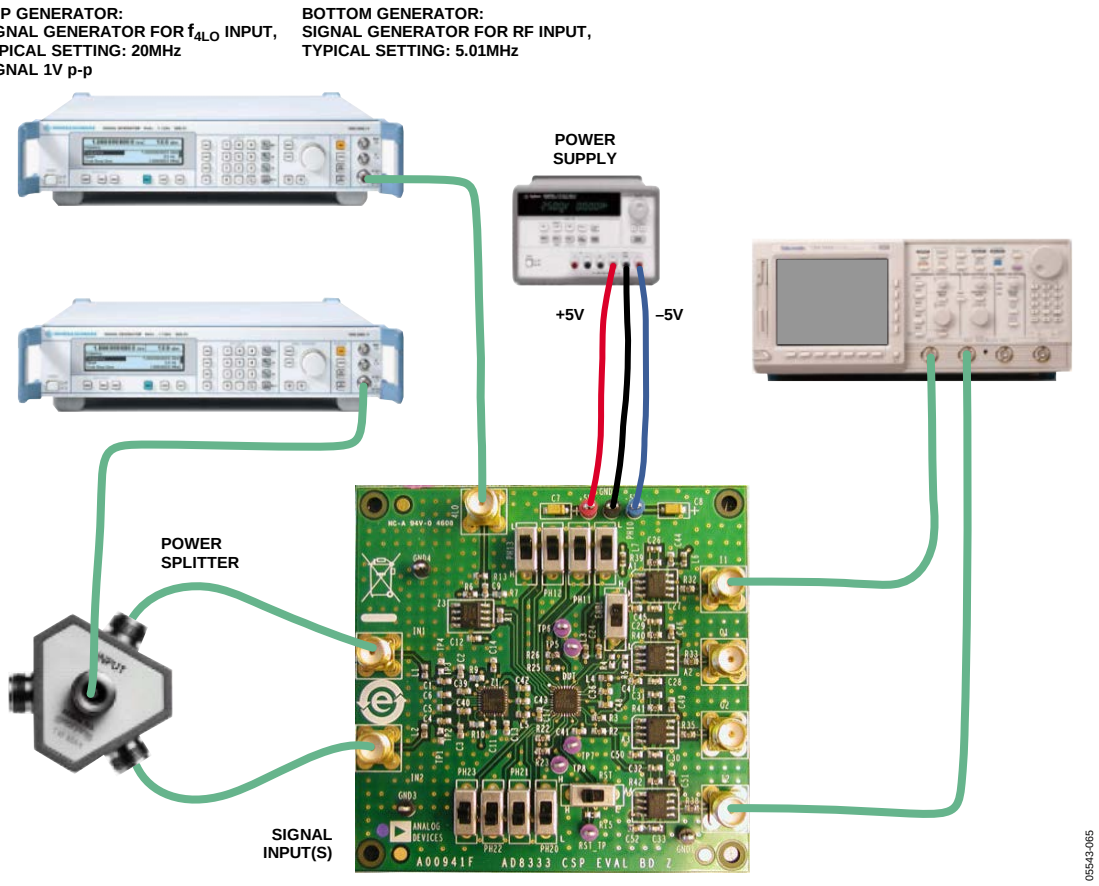


Figure 65. Typical Board Test Connections (One Channel Shown)

BOARD LAYOUT

The AD8333 evaluation board has four layers. The interconnecting circuitry is located on the outer layers with the inner layers dedicated as power and ground planes. Figure 66, Figure 67, Figure 69, and Figure 70 illustrate the copper patterns.

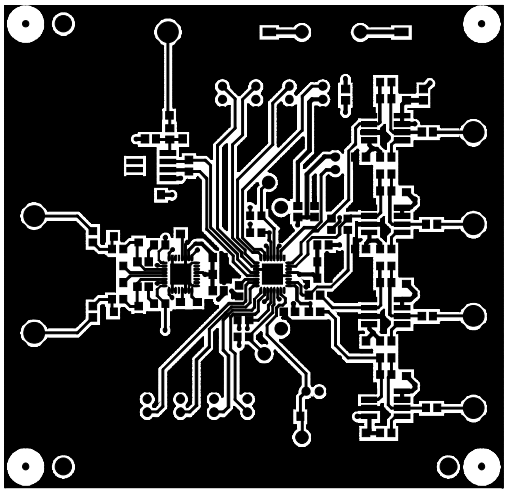


Figure 66. Component Side Copper

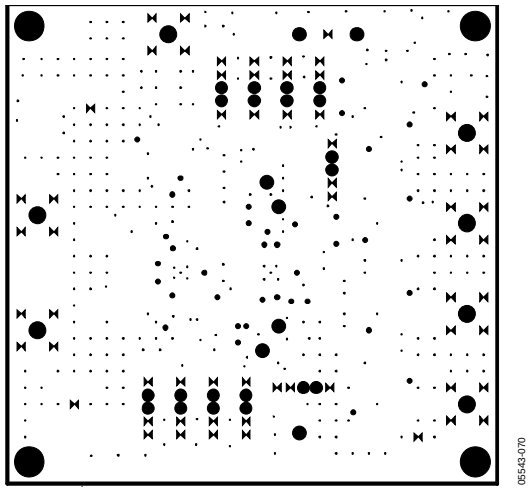


Figure 69. Ground Plane Copper

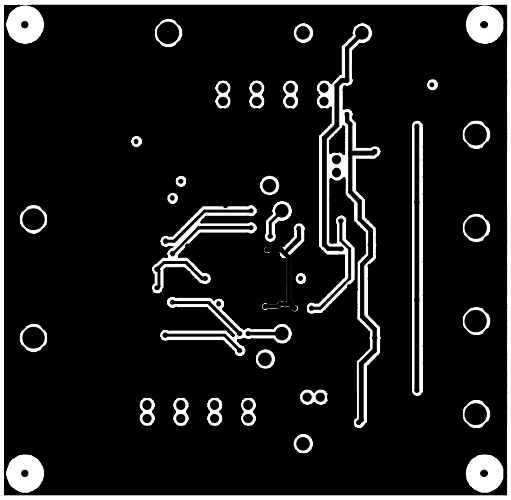


Figure 67. Wiring Side Copper

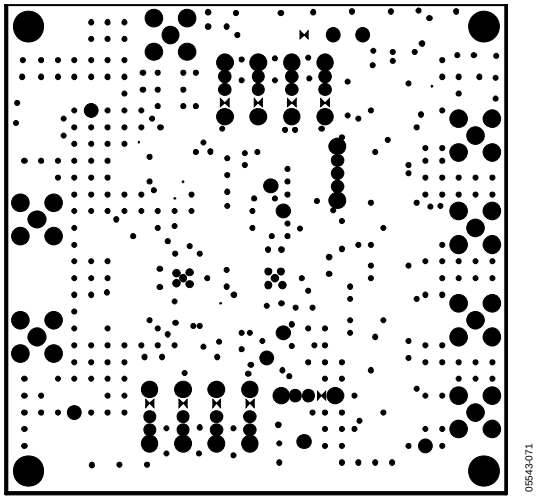


Figure 70. Power Plane Copper

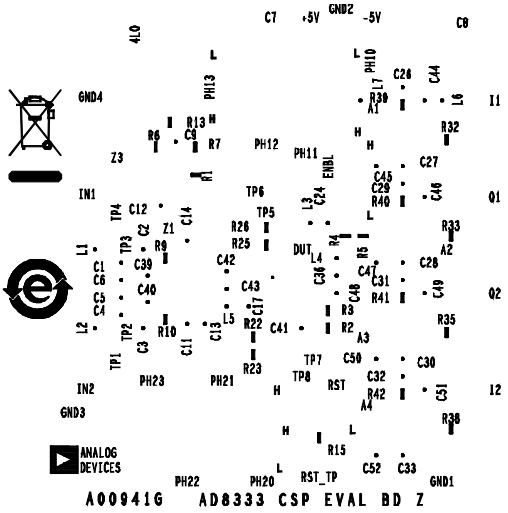
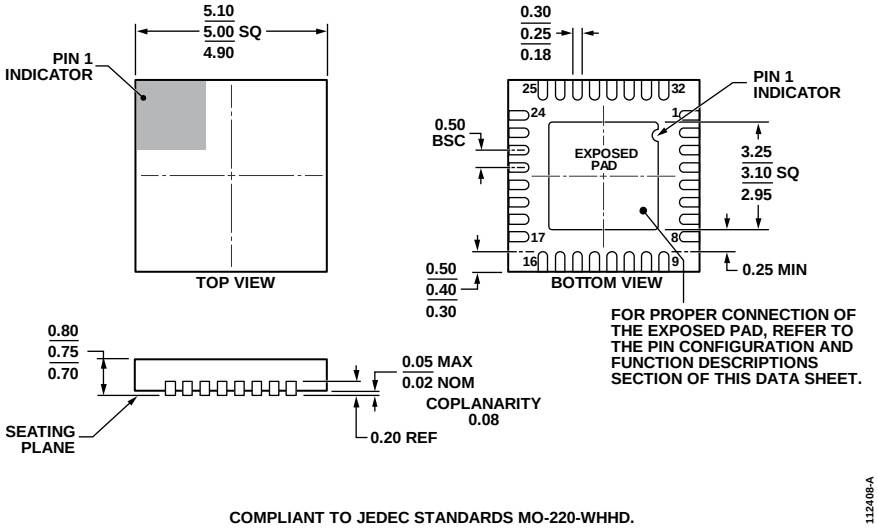


Figure 68. Component Side Silkscreen

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WHHD.

Figure 71. 32-Lead Lead Frame Chip Scale Package [LFCSP]
5 mm × 5 mm Body and 0.75 mm Package Height
(CP-32-7)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Package Option
AD8333ACPZ-REEL	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP]	CP-32-7
AD8333ACPZ-REEL7	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP]	CP-32-7
AD8333ACPZ-WP	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP]	CP-32-7
AD8333-EVALZ		Evaluation Board	

[1] Z = RoHS Compliant Part.
[2] WP = waffle pack.